Reprinted from

# Eighth International Symposium

# Machine Processing of

# Remotely Sensed Data

with special emphasis on

# Crop Inventory and Monitoring

**July 7-9, 1982**

# Proceedings

Purdue University
The Laboratory for Applications of Remote Sensing
West Lafayette, Indiana 47907 USA

# DEVELOPMENT OF A HIGH SPEED IMAGE PROCESSING SYSTEM: TIAS 3000

H. SHIMODA, I. FUJITAKA,
K. FUKUE, T. SAKATA

Tokai University
Tokyo, Japan

## I. ABSTRACT

In the last decade, several kinds of specialized image processors have been discussed and some of them were realized. They were mostry designed for generally increasing the processing speed or for special jobs, but there are none for operational data processing of remote sensing.

On the other hand, coming earth observation satellites in the next 10 years will be installed with high resolution sensors. These sensors will bring 200-1000x$10^6$ bytes of information for a scene, which is about 10 times of the existing remotely sensed data. Furthermore, these resolution increasement will require more sophisticated processings, especially spatial information handlings which will increase the processing quantity to 10 times of the existing systems.

In order to achieve operational processings of these kinds of data, new type image processors should be developed. TIAS(Tokai Image Analysis System) 3000 is now under development to meet this requirement.

TIAS 3000 is composed of four subsystems. They are 1)high resolution display, 2)high speed arithmetic processor, 3)mass buffer memory, and 4)controller. It is intended to achieve interactive image processing tasks of remotely sensed data with aid of the host general purpose image processing system TIAS 2000[1]. It can slso be used for other kind of tasks, e.g. annimation, three dimentional display, motion picture analysis, etc, which needs very high speed processings.

As a conclution, TIAS 3000 will be one of the fastest image processor in the world and can meet the requirements of comming era of operational remote sensing data processings.

## I. INTRODUCTION

In the last decade, many kinds of digital image processing systems were developed. Performances of these systems are increasing year by year. The strongest requirements for the performance of image processing systems come from the field of remote sensing. Images taken by LANDSAT series MSS contain about 7x$10^6$ pixels. Images which will be taken by earth observation satellites which will be launched during coming 5 years will contain 30-100x$10^6$ pixels for one scene. These amounts of pixels correspond about 200-1000x$10^6$ bytes informations. Another kind of data sources which also brings similar amount of informations are aerial photographs. They contain about 180-640 x $10^6$ bytes for one scene.

Suppose to classify these images by a maximum likelihood classification. Maximum likelihood classifications require about 500 floating point operation for one pixel in order to classify 36 categories from 4 bands images. In order to depress the total processing times for one scene in a reasonable period (may by 1-2 hours), one floating point operation should be less than 100 nsec. Desirable speed will be about 10 nsec. Furthermore, it will be very difficult to increase classification accuracies for these high resolution images(may be 10-30m ground resolution) if one use only point wise processings. Spatial processings such as a texture analysis will be necessary for these images, which largely increase the performance reuqirements of image processing systems.

It is not impossible to use general purpose computers for such a purpose. Some of them which are usually called

super computers already cleared these requirements. However, from the viewpoint of operational remote sensing, they are too much expensive.

These discussions above strongly suggests developments of special purpose processors for image processings of operational remote sensing in near future. There are several kinds of commercially available systems which are called specially designed image processing systems. However, most of them are mainly image displays and have limited capability of image processings.

This paper describes the design of microprogrammable high speed image processing system TIAS 3000 which is under development in Tokai Research & Information Center, Tokai University.

## II. SYSTEM REQUIREMENTS

There are many kinds of high speed processors which were built for general purpose computer systems. Some of the architectures of these processors can be utilized in image processing systmes. However, there remain some problems which are intrinsic for image processings. Requirements which are caused by these problems are discussed below.

### A. INTERACTIVE PROCESSINGS

Most of the image processing tasks are done interactively now. It is because human abilities for pattern recognition for exceeds machine abilities. The main part of man-machine interfaces in image processings is an image display. Information amounts which are necessary for image displays are so much that it takes too much time for data transfer if data processors and a display is seperated. This problem requires the data processors for image processings to be directly connected to the buffer memories for display. This architecture also assures that data feedings to the processors can be very fast.

### B. HIGH QUALITY DISPLAY

Most of image displays which are used in image processing systems are composed of about 500x500 pixels. Image qualities of this kind of displays are not enough for human perception. The minimum requirement will be 1000x1000 pixels. This image size determines the minimum scale of buffer memories. The data transfer efficiency between the buffer memories and mass storage units also depends on the buffer memory size. The larger the memory, the better the efficiency.

The second problem for the buffer memory is its bit depth of each pixels. The minimum requirements for color image display only are 4-5 bits for 3 principal colors. However, as a buffer memory for high speed processors, the original bit pattern should be conserved. Remote sensing images are usually multi channel images composed of 8 bits unit. The maximum channels of satellite images which are main targets of this system will be 7 channels of Thematic Mapper of LANDSAT-D. In order to store the results, the minimum requirement will be 64 bits for each pixel.

### C. HIGH SPEED PROCESSOR

There are many kinds of processings in image processings. Some of them are integer calculations, while the others are floating point calculations. Some of them are address dependant, some of them are not. If this system is composed of only one processor, it should perform many kinds of operations, which will decrease its efficiency. It will be better to install many kinds of single purpose processors.

The target data can be devided into four categories. The first one is pixel wise operations which are most popular in remote sensing data processings. The second one is local operations such as spatial domain convolutions. The third one is global operations such as Fourier filterings. In the last case, the target of operations is not data itself, but addresses of data, e.g. geometric corrections. In order to process local operations efficiently, data in each local area should be accessed simultaneously, and for the 3rd and 4th type operations, some kind of address processors would be necessary.

### D. FLEXIBILITY

Image processing algorithms in remote sensing had not yet been established. Especially local and global processings are in the research stage. In order to adopt future algorithms, the system should be flexible.

TIAS 3000 was designed to meet the above requirements.

## III. OUTLINE OF TIAS 3000

Fig.1 shows the block diagram of TIAS 3000.

The system function is devided in 5 subsystems. They are 1)high resolution display, 2)high speed processor units, 3) mass memory which are common for both above units, 4)microprogrammable intelligent system controller and 5)front end processor which is an interface to periferals and the host system.

High resolution display is a color display which has about 1000x1000 resolution. It has also character and graphic functions and controlled by image display controller.

High speed processor units are composed of 3 units. They are function memories, an ALU array(array processor) and pipeline processors. The first one is mainly used for one to one data conversions. The second one is mainly designed for local operations and the last one is used for floating point operations. The floating point processing unit can be multiple. The speed of the array processor is about 300 MOPS and the speed of the pipeline processor is about 8-32 MFLOPS in an ideal case.

Buffer memory is 10M bytes(1024x1024x8 x10 bits) and the system is controlled by microprogrammable control processor made of bit slice microprocessors.

The front end processor is a HP-2113E which has a compatibility with the computers of the host system and composes a local network.

## IV. FUNCTIONS OF EACH SUBSYSTEM

### A. BUFFER MEMORY

The buffer memory is composed of an image part and a graphic part. Image part is composed of 8 planes, each of which is composed of 1024x1024 pixels, and 8 bits for each pixel. These memories can be used as eight 8 bits planes or four 16 bits planes or two 32 bits planes or one 64 bits plane. Graphic part is composed of 16 planes of 1024x1024 pixels, 1 bit plane. These graphic planes can not only be accessed independently, but also can be used as two 8 bits planes.

### B. BUS CONFIGURATION

Four kinds of buses are used in this system. Table 1 shows their speed, bit width and purposes.

### C. MEMORY I/O

Fig.2 shows the block diagram of memory I/O system.

The highest memory access speed was defined to be 17 nsec/pixel from the data transfer requirement to the high resolution display. In order to achieve this speed, 16 fold parallel read out are done and read data are multiplexed and fed to the D bus.

The most distinctive feature of this memory I/O system resides in its address control processor. I can generate not only several kinds of special addressings for displays (i.e. zooming, windowing, shrinking, etc.), but also addresses for real time image processings by storing addresses in address pattern memory.

For instance, in two dimensional FFT, the butterfly addressing and corner turning can be automatically achieved in real time, which largely increases the processing speed.

### D. HIGH SPEED PROCESSORS

As has been mentioned before, high speed processors are composed of function memories, ALU arrays and floating point processors. Function memories are used as look up tables. It's confiquration is 16 bits input 16 bits output, i.e. 128K byte, and works in P bus speed.

Fig.3 shows a standard confiquration of ALU array processor. This processor is composed of nine 8 bits multipliers, nineteen 16 bit ALU's and parameter memories for constants. The input data are provided from multi line buffer in P bus speed and mainly used for local operations like spatial convolutions. This ALU array can also be reconfigured for another kind of operations.

The floating point processors are pipelined processor with 32 bits input and 32 bits output. This processor is mainly used for floating point operation like FFT or maximum likelihood classifications. Multiple processors(8 maximum) can be installed in this system to increase the operating speed.

### E. DISPLAY

Image output is usually displayed on 1000 lines high resolution display, but in order to interface conventional video systems such as video tape recorder, TV camera, etc., it has 4 output modes as shown in Table 2. The image output modes on display is shown in Table 3.

In order to display ancillary data of the images, there are side zones on both sides of the image display area. Alpha-numeric data and color codes can be

displayed here. Characters can be displayed also on the image area. Each character display specification is shown in Table 4.

The images are displayed through three planes of function memories(8 bits input/ 8 bits output). Therefore displayed colors can be controlled in real time independent from image processings. In order to achieve interactive processings of such works, an operation console is attached to the system. Functions which can be achieved on the operation console are shown in Table 5.

F. CONTROL

The controls of each processors in the system are done by microprogrammable controller made of bit sliced micro processors. Microprograms are stored in ROM or WCS(Writable Control Store).

Front end processore(HP-2113E) does 1) total system control, 2)rewrite to function memories and parameter memories, 3)peripherals control, and 4)interface to the host system.

## V. CONCLUSION

The advantages of TIAS 3000 are summarised below.

1. Very high processing speed can be achieved by the introduction of multi processor for each purpose.

2. Spatial processings can be performed very efficiently by the introduction of address controller and multi line buffer.

3. Hyper-speed display, high speed parallel operations and low speed general purpose processings can be done simultaneously by configuring hierarchical bus architecture.

4. It is very flexible by the adaptation of microprogrammable controllers.

5. Large image data up to 8M bytes can be processed at me one time.

6. Although high resolution display is utilized, it has an interface to conventional video systems.

7. Interactive processings can be achieved in real time using switch or volumes on the operation console.

## VI. REFERENCES

1) K.Fukue,H.Shimoda and T.Sakata,"A Development of Interactive Image Processing Software System TIPE", Proc. 7th Inter. Symp. on Machine Processing of Remotely Sensed Data,p158-168 (1981)

## AUTHOR BIOGRAPHICAL DATA

Haruhisa Shimoda recieved the Ph.D. degree in solid state physics of Organic semiconductor from the University of Tokyo, Tokyo, Japan, in 1972. Since 1972, he has been an Assistant Professor of the Department of Electro Photo-Optics Enginering at the Tokai University, Kanagawa, Japan. He is currently engaged in field of digital image processing, a development of image processing system, and application of digital image processing to remote sensing.

Ichiro Fujitaka was born in Zushi, Japan in 1944. He received his B.S. E.E. degree from Tokyo Institute of Technology at Tokyo in 1967. Then he joined Nippon Electric Company(NEC) and has been working in LSI development. He is now the manager of the department of custom LSI development. He is also a member of Tokai University Reaearch and Information Center since 1977. He has been mainly engaged in developments of image input and output systems there.

Kiyonari Fukue recieved the B.S. and M.S. degrees from the Tokai University of Kanagawa, Japan, in 1976 and 1978, respectively. From April 1978 to March 1981 he was a graduate student of doctor cource in the Department of Electro Photo-Optics Enginering, Tokai University. Currently, he is an assistant at the Institute of Research and Development, Tokai University. His research interests include digital image processing and system, especially in remote sensing.

Toshibumi Sakata recieved B.S. degree of Chemical Enginering from Chiba University. He took doctor in Enginering of Chemical Physics at the University of Tokyo and then joined to the Institute of Industrial Sciene there, as a research associate. He was a research scientist of Munich University during 1964 to 1966. In 1966 he moved to the Tokai University and he had a chair of professor in 1971. Presently he is the director of Tokai Research and Information Center, the Tokai University.

Table 1 Bus Specifications.

| BUS | SPEED | BITS | USE |
|---|---|---|---|
| D | 17 ns | 40 | DISPLAY |
| P | 60-70 ns | 80 | INTEGER OPERATION |
| CPU | 500 ns | 80 | FLOATING POINT OPERATION |
| CNTL | 500 ns | 16 | DATA CONTROL I/O |

Table 2 Display Output Mode.

| | LINES/FLAME | FLAME/S | FIELDS/S | INTERLACE |
|---|---|---|---|---|
| 1. | 1125 | 30 | 60 | 1/2 |
| 2. | 1125 | 15 | 60 | 1/2 |
| 3. | 563 | 60 | 60 | NON |
| 4. | 525 | 30 | 60 | 1/2 |

Table 3 Image Output Mode.

| | | |
|---|---|---|
| 1. | 1024 x 1024 | pixels |
| 2. | 1024 x 1024 | pixels |
| 3. | 512 x 512 | pixels |
| 4. | 512 x 480 | pixels |

Table 4 Character Display Specification.

| | |
|---|---|
| SIDE ZONE | 85 x 512 DOTS<br>12 x 56 CHARACTERS |
| FULL AREA | 97 x 56 CHARACTERS<br>B/W CHARACTER |
| COLOR CODE | 56 COLORS |

Table 5 Function of the Operation Console.

1. MONITOR CH. SELECT
   0-7 ch to R,G,B
2. COLOR BIAS
   R,G,B Analog (Digital Read Out)
3. COLOR GAIN
   R,G,B Analog (Digital Read Out)
4. ZOOMING
   Hardware Control x2 x4 x8 x16
   Scroll
5. ZOOM POINTER
   Joistic
6. CURSOR
   + Mark
   Track Ball Control
7. HISTGRAM
   R,G,B or 1 ch (R+G+B)
   256 Levels(8 bits) x 16M counts(24 bits)
   Histgram Cursor (Line,Window)
8. WINDOW
   Window Setting by Cursor
   Automatic Hold of Window (Hardware Control)
   Masking
   Blinking
   Sampling

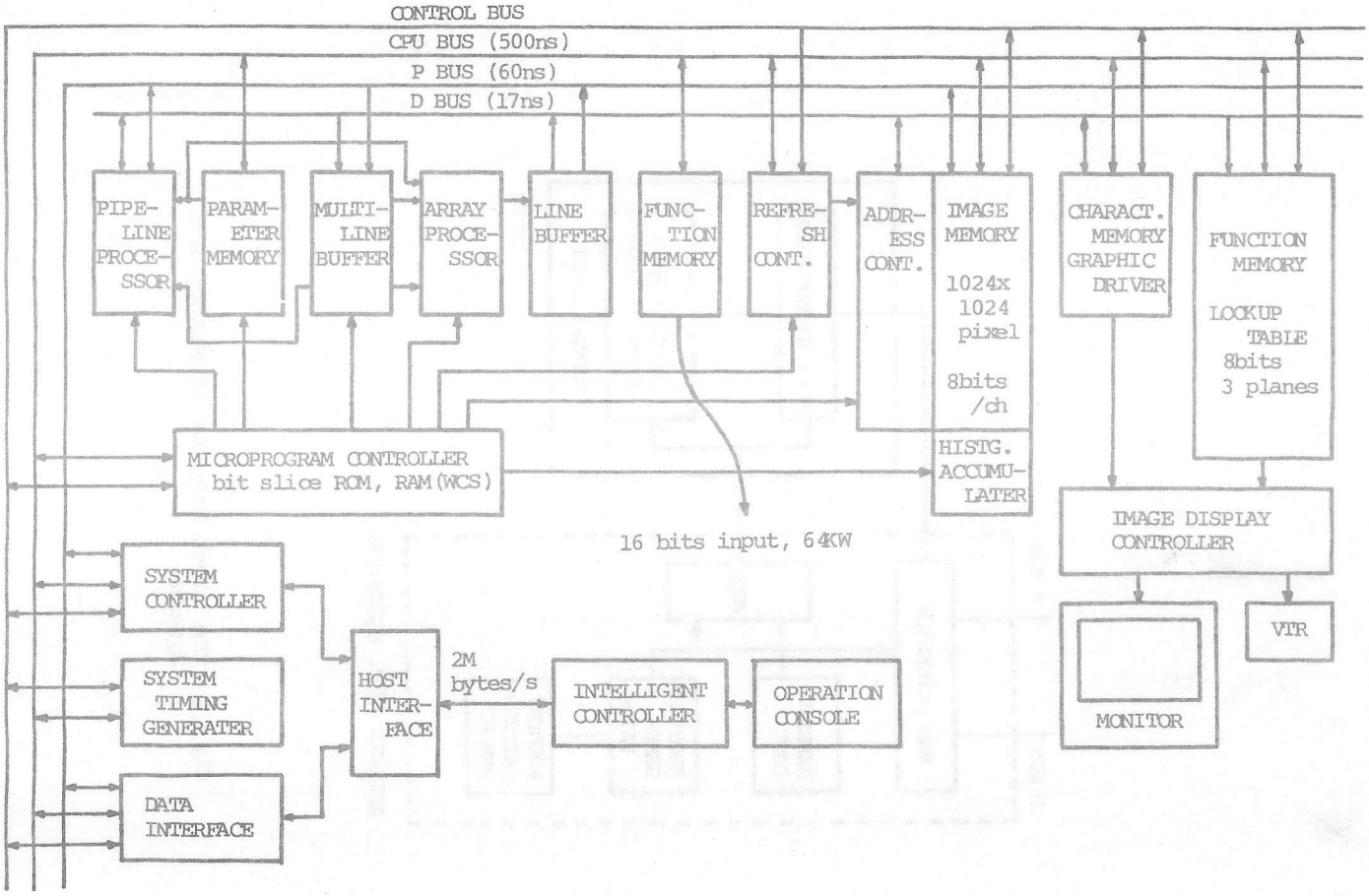


Fig. 1 The Block Diagram of TIAS 3000.

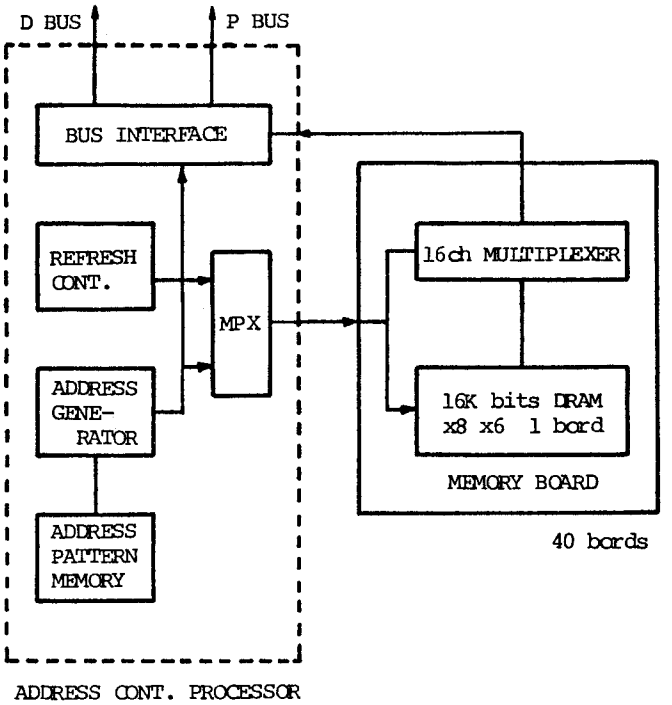


Fig. 2 The Block Diagram of Memory I/O System.

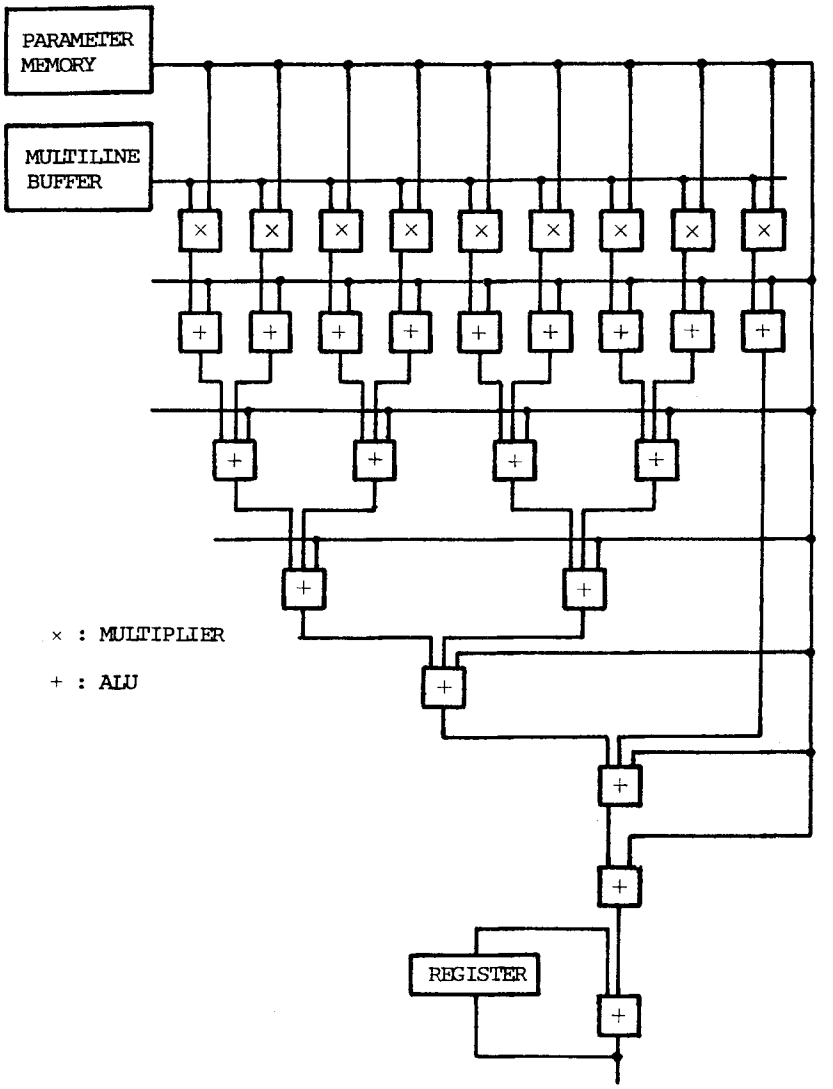


Fig. 3 A Standard Configuration of ALU Array Processor.