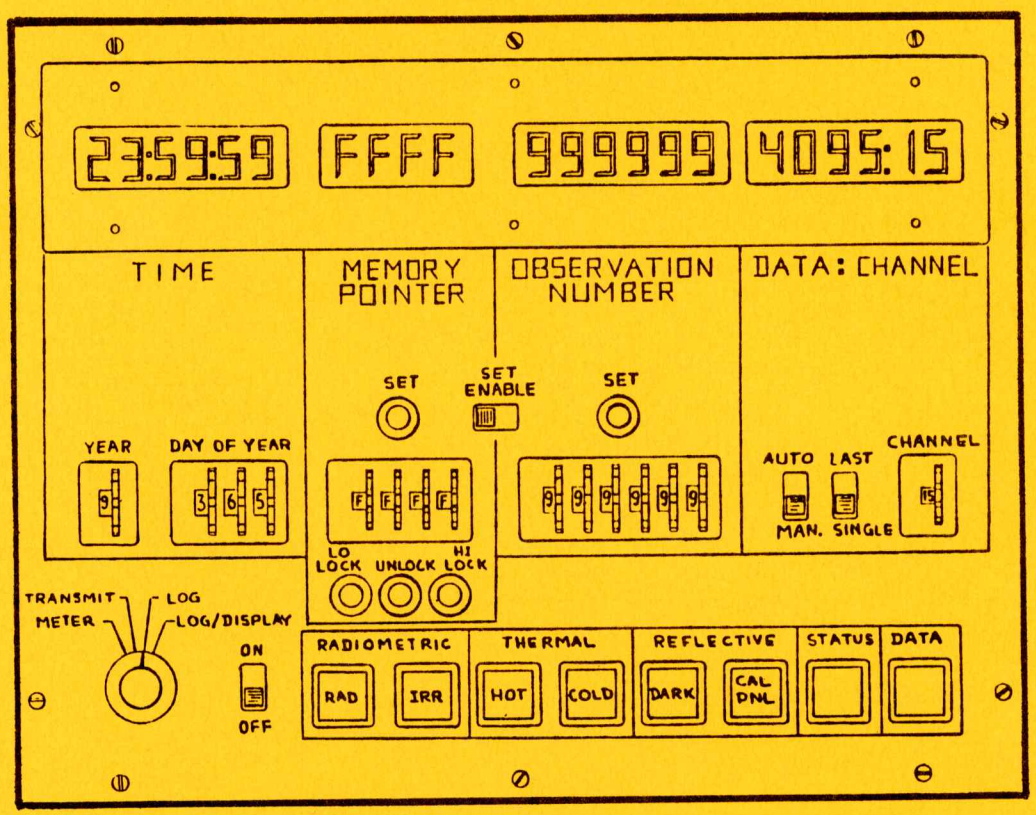
LARS Technical Report 070181

The Design and Construction of a Special Purpose Data Logger

by

Michael K. Stabenfeldt



Laboratory for Applications of Remote Sensing
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1981

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Michael K. Stabenfeldt

July 1981

ACKNOWLEDGEMENTS

I would like to thank Professor Silva for his assistance throughout the project. I would also wish to thank Barrett Robinson for designing the chassis and his assistance when I needed it. Without these two people, the project would have been impossible for me.

TABLE OF CONTENTS

LIST OF FIGURES

ABSTRACT

Stabenfeldt, Michael Karl, M.S.E.E., Purdue University, August 1981. The Design and Construction of a Special Purpose Data Logger. Major Professor: L. F. Silva.

A Data Logger for field data acquisition, utilizing CMOS technology, was designed and constructed. The logger is part of a spectral data acquisition system used in Remote Sensing field research. The Data Logger was designed for field use with a Barnes Engineering model 12-1000, multiband radiometer. The unit was functionally tested and evaluated. Preliminary designs for a second-generation instrument were also completed.

INTRODUCTION

Basic Measurement System In Use

The primary intent of the measurement area at the Laboratory for Applications of Remote Sensing (LARS) is to measure the bidirectional reflectance factor for crop canopies. What is in fact measured is the biconical reflectance factor. Due to the small size of the detector aperture in relation to the distance from the target to the detector aperture, the biconical reflectance factor closely approximates the bidirectional reflectance factor. See reference 1 for a complete discussion of the bidirectional reflectance factor. The bidirectional reflectance factor is defined as the ratio of the radiance from the target to that from a reflectance standard, taken under identical conditions of illumination and viewing. Practically, the factor is computed by taking the radiance from the target, subtracting the dark level signal, and dividing this quantity by the radiance of the standard minus the dark level. The result is almost correct. Since the standard is not a perfect reflector, the previous result must be multiplied the standard's real reflectance, which

is on the order of 90 to 95 percent for the field standards used at LARS. Thus to measure the bidirectional reflectance factor of a scene, it is necessary to rapidly measure so the sun angle does not vary too much, the standard and the target from the same viewing angle. In addition, the dark level must be measured. Presently, the standard is measured at roughly 15 to 20 minute intervals. The dark level, which is a function of the electronics and detector, have been found to be fairly stable. The dark level is still measured approximately every 30 minutes to an hour, to account for and locate any system problems.

It is important that the source of illumination be constant. In the case of a field measurement, this implies a relatively cloud-free sky. A passing cloud may not block the sun from illuminating the scene, but it can change the incoming radiance level. Thus it is important to watch for clouds that pass near the sun. Finally, we have found that it is impossible to obtain valid data on an overcast or very hazy day. Illumination is not stable enough to obtain repeatable data.

Model 100 Data Acquisition System

One of the current spectral measurement systems at LARS consists of an Exotech model 100 radiometer, a Barnes PRT-5 thermal radiometer, an air temperature probe, and a data logger. The Exotech model 100 has four spectral bands

located in the visible and near infrared wavelength regions. The PRT-5 measures the surface temperature of the target. The air temperature probe, a bead thermister, measures the air temperature directly above the crop canopy. All of these analog sources are connected to the data logger. A data logger was constructed at LARS several years ago for use with the model 100 radiometer. It uses a three-and-one-half digit digital voltmeter (DVM) in conjunction with a printer for hard copy of the data. The paper output of the data logger requires the data to be keypunched before it can be analyzed and stored in the computer system.

Philosophy Of An Eight-Band Radiometer

The LARS measurement area has, for a number of years, been collecting spectral data with the model 100 system and with another much more complex instrument, the Exotech model 20C radiometer. There are a number of differences between these two systems. The largest difference is that the model 20C is a scanning radiometer. An optical filter, a circular variable filter to be precise, is rotated in the optical path of the detectors. The output of the detectors are recorded on magnetic tape and on a chart recorder. Once suitable corrections as described in the first section are performed, the bidirectional reflectance factor can be computed for the target from roughly .4 micrometers to 2.4 micrometers. The model 20C provides

fine wavelength resolution of the target reflectance factor, but the instrument is difficult and expensive to use in the field. The instrument is very large and bulky, requiring a hydraulic boom to extend the instrument over the target field. The instrument requires a large amount of support electronics, which are housed in another vehicle. These electronics require a generator to power them. The expense of operating the system is high in terms of manpower to collect the data and computer time to analyze the data. The initial capital expenditure is large too. The final disadvantage of the model 20C is its slow speed. The model 100 system can collect data over 250 test fields in a day. The model 20C can only collect data over about 80 fields in the same time.

Because of the large costs and slow speed of the model 20C, a new system was proposed that would keep the advantages of the model 100 system, but expand the spectral data collected into the middle and thermal infra-red spectral regions and increase the resolution in the visible and near infra-red spectrum. The bands would cover spectral regions which had been deemed important to remote sensing by earlier research with instruments like the model 20C. An eight band unit was felt to provide adequate resolution. The bands selected were the thematic mapper bands plus a band from 1.15 micrometers to 1.3 micrometers. In addition, a data logger would be designed to

interface with the radiometer for very rapid collection of data.

Initial Requirements Of The Data Logger

The initial design goals for the data logger were it must be

1. rugged, lightweight, and portable,
2. battery operated,
3. relatively low cost (under $10,000),
4. parallel multichannel analog input port compatible with analog outputs of radiometer,
5. at least one digital input channel for ancillary data,
6. simultaneous sample and hold for each detector channel,
7. small meter for input quality verification,
8. provision to enter date, time and observation number,
9. digital hard copy printer output to tabulate data values for each radiometer channel, plus ancillary data,
10. parallel, multichannel buffered analog output of analog input channels,

11. digital data output channel compatible with both punched paper tape and digital cassette tape recorders,

12. auxiliary analog input ports with adjustable gains to accommodate signals from thermal sensors such as the Barnes PRT-5,

13. Conversion accuracy of .05 percent.

Procurement Of Instrument

The National Aeronautics and Space Administration (NASA) contracted with LARS to obtain quotes for the proposed eight band radiometer and matching data logger. Several manufacturers were contacted and given detailed requirements for both instruments. Only one manufacturer bid on these proposed instruments, Barnes Engineering. While the bid for the radiometer was considered acceptable, the data logger bid was considered excessive. Since no other manufacturers were willing to bid on the data logger, LARS decided to design and build the unit internally. The responsibility of the production of the prototype was given to the author.

Revised Specifiactions For The Data Logger

In the time period from searching for a manufacturer to build the data logger and the decision to build the logger at LARS, some of the basic design goals of the

instrument were changed. The most dramatic change was the concept of storing data in static random access memory (RAM) as opposed to hard copy printer output. Static RAM offers unmeasurably low bit storage errors, so it was felt to be a viable storage medium. In addition, several RAM manufacturers had just introduced products which consumed very little power while storing 4096 bits per package. Hence there could be a real power saving by using RAM as opposed to a printer. The RAM also offers convenience in transferring the data directly to the computer as opposed to keypunching the paper tape output. Eliminating the keypunching reduces the likelihood of an error in the data transfer too. The final advantage of the RAM is that an observation could be recorded much more rapidly. This implied that the sample and hold circuits on the analog inputs could be eliminated.

Several other less major changes in the design goals were made to simplify the circuitry or eliminate options which were felt convenient, but not absolutely necessary. The digital input port was eliminated due to its limited immediate use. The parallel multichannel buffered analog outputs of analog inputs was eliminated. This feature would have required an array of amplifiers that would consume extra power. The auxiliary analog inputs do not have adjustable gains. Here again, this would have required an additional amplifier for each auxiliary analog input.

Instead, it was felt the sensor electronics could be modified to have the same dynamic range as the eight band radiometer, zero to five volts. Wider dynamic ranges can be reduced with the addition of a resistive divider. Lower dynamic ranges would require an external amplifier, or if twelve bit accuracy is not required, simply measure the analog source with less accuracy. A source that can have negative outputs must utilize an external amplifier.

Features that were added to the data logger were the ability to interface with a HP-97S calculator, a HP-85 micro-computer, or a computer such as the PDP-11/34. The unit was designed to have a field replaceable memory module in the event the current module was filled. Finally, the data logger was designed to interface with a camera display unit, also designed and built at LARS.

DESIGN OF CIRCUITS

Introduction

In this phase of the project, a system design of the data logger was proposed that would implement the desired features of the proposed data logger. After the system design was completed, individual blocks of the data logger were designed at the gate level. During this phase, consideration was given to the availability of a component before the component was specified.

In this section the system design is described followed by descriptions of the subcircuits designed to implement each system block.

System Design

Shown in figure 1 is the block diagram for the data logger. The block diagram shows several design decisions that were made early in the project. The first was the use of a hardwired controller as opposed to a microprocessor. This decision was made due to the higher speed performance obtainable from a hardwired controller as compared to a microprocessor and its lower power consumption. The second

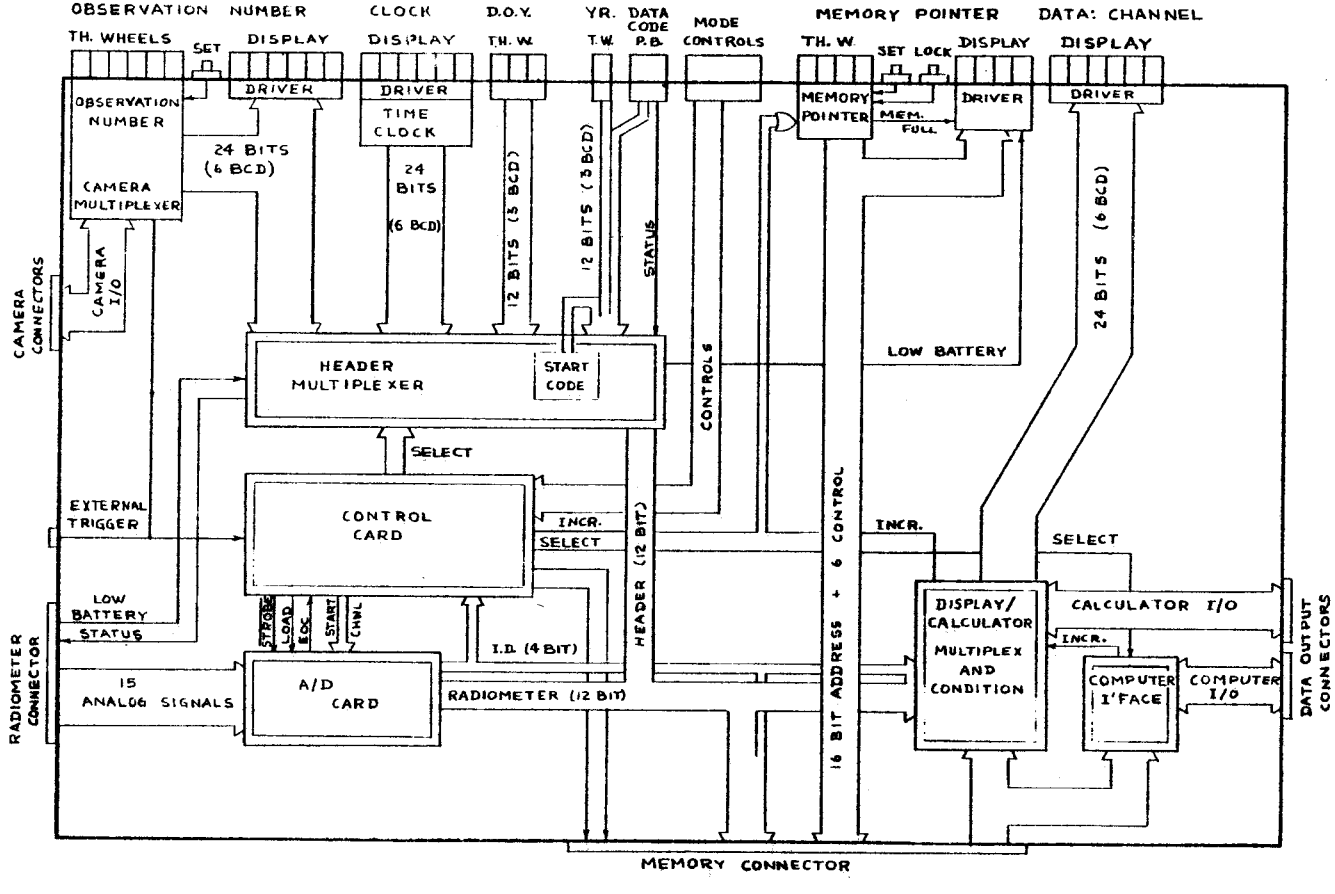


Figure 1. System Block Diagram

was the use of a commercially available data acquisition module as opposed to buying a analog multiplexer, amplifier, and analog-to-digital converter separately. A unit from Analogic (model DM6812) was chosen due to its speed and low power consumption. The unit incorporates a 12-bit analog-to-digital converter with a 16 channel multiplexer. A 12-bit converter accuracy was chosen since the primary data source (the multiband radiometer) has a .1% accuracy. A 12 bit converter will provide $\pm$.025% resolution. With all sources of inaccuracy considered, the Analogic module maintains $\pm$.05% relative accuracy. This was felt to be adequate.

The third early design decision was the choice of the data storage format. Shown in figure 2 is the format that was chosen. The basic scheme uses a memory word that can consist of one of two types of data. The first is digital data which consists of three Binary-Coded-Decimal (BCD) digits followed by four zero bits. The second type of data is analog-channel data. This consists of a 12-bit full binary representation of the channel data followed by the channel number in full binary. This scheme, while not being the most efficient, offers three advantages. First, it is possible to identify the beginning of a new observation no matter what preceded it. This is possible since the start code is chosen to be greater than a BCD '9'. In this way, any memory location consisting of the start

LOCATION	VALUE	BIT 0
N	START | YEAR | TYPE	0000
N+1	DAY OF YEAR	0000
N+2	UPPER HALF; TIME	0000
N+3	LOWER HALF; TIME	0000
N+4	UPPER HALF; OBSV	0000
N+5	LOWER HALF; OBSV	0000
N+6	CHAN. 1 DATA	0001
N+7	CHAN. 2 DATA	0010
N+8	CHAN. 3 DATA	0011
N+9 • • • •	• • • • •	0100
N+20	CHAN. 15 DATA	1111
N+21	START | YEAR | TYPE	0000

Figure 2. Storage Format

code, any 8 bits, and four zero bits (total of 16 bits) is the beginning of a new observation. The next five memory locations should all contain three binary coded decimal digits followed by four zero bits. If this is not the case, there is an error in the data. Following these locations, the upper 12 bits are arbitrary. The lower four bits will be arranged in one of two ways. Either they will start at 1_{16} and continue up to at most 15_{16} (as shown in figure 2), or contain a single channel. In both cases, the data will be followed by another start code. This redundancy leads to the second advantage of this encoding scheme; namely it is easy to detect errors in the data storage process, and in many cases correct them. The third reason for using this encoding scheme is that it provides easy decoding of the data for displaying the data to the operator or interfacing to an external HP-97s calculator. The decoding scheme reduces to checking the lower 4 bits of data. If they are all zero, then the data is displayed as three BCD digits on the left side of the data display, with 00 on the right side of the display. If the lower 4 bits of data are not all zero, then the upper 12 bits of data are decoded into their base 10 equivalent representation, and displayed on the left side. The lower 4 bits of data are decoded into their base 10 representation and displayed on the right side.

The remaining major system blocks include a time clock which reverts to internal batteries when the data logger is off, an observation counter which is automatically incremented after each observation is completed, a controller, a camera interface, a computer interface, a radiometer interface, a memory pointer, a memory module, a data decoder/calculator interface, a digital multiplexer, and a data acquisition module.

Bus Structure And Interconnect

Figure A-1 shows a general interconnect layout for the data logger. Not all details are shown for clarity. Each block represents a single board or set of printed circuit boards that perform a given function. The output from the A/D board and MUX board are on the same bus. This bus drives the memory module input and one of the inputs on the calculator interface board. The memory address block feeds the memory module directly. No other circuitry needs the memory address information. The output of the memory module drives the computer interface and the second input of the calculator interface via connectors JC2/JCA2. The data display is driven from the output of the calculator interface. The MUX board derives its inputs from the time clock, observation counter, and front panel circuitry. The controller is responsible for tying all of these boards together. Because of the non-microprocessor approach to the problem, to obtain a good feel for the

system, one must examine each subsystem first, and then return to the interconnect layout and the block diagram.

Radiometer Interface

The Barnes radiometer has eight analog outputs which measure the seven Landsat D Thematic mapper spectral bands plus a 1.15 micrometers to 1.3 micrometers. These outputs are normally the first eight analog inputs to the data logger. Additionally, the radiometer has three analog outputs which measure various temperatures within the radiometer. These include the chopper temperature, cavity temperature, and the frame temperature. These are channels 9, 10, and 11 respectively. All eleven of these outputs are pseudo-differential outputs to prevent ground loop problems and maintain good noise immunity.

The radiometer in addition to eleven data channels, contains a digital input and a digital output. The digital output indicates when the input power supply voltage has fallen below a usable voltage. This indicates the battery should be recharged before more data is collected. The output consists of an opto-isolator as shown in figure A-2. A circuit (also shown in figure A-2) was designed to use this output to drive a colon indicator on the memory pointer display when the battery is sufficiently charged. If the colon is not visible, then this is an indication of a low battery. The circuit shown is very rugged as well as

sensitive. It requires that the opto-isolator in the radiometer provide a voltage drop of no more than 2 Volts at .5 milliampere. The circuit in the data logger utilizes a opto-isolator at the front end. This provides that any input voltage on these terminals cannot damage any component beyond the opto-isolator. For high sensitivity, a Texas Instruments 4N49 opto-isolator was chosen. The unit claims a current transfer ratio of 800%. The output photo-transistor was driven in an emitter follower configuration that fed a schmidt-trigger input CMOS inverter. A schmidt-trigger input was used to obtain improved noise suppression and lower power consumption. If a normal buffer was used, power consumption would increase since the output of the opto-isolator will swing to the power supply rail when the opto-isolator is conducting. With normal CMOS gates, the closer the input voltage of the gate is to either V+ or ground, the lower the quiescient current of the gate.

The output of the inverter is then exclusive or'ed with a 60Hz square wave to properly drive the LCD segment.

The input to the radiometer is used to control an internal multiplexer in the radiometer. If the input is left floating, the normal spectral data is presented to the data logger. If the input is shorted to its return line, then the output voltage presented by 7 of the 8 spectral data channels in the radiometer are determined by

the gain setting of the respective channel. Thus the gain of each channel can be queried or stored for future reference. The 8th channel is the thermal channel which has only one gain setting. The circuit used to accomplish this function is also shown in figure A-2. Again an opto-isolator was used. In this case, opto-isolation was essential to keep any current from flowing through the analog return wire between the radiometer and the data logger. The opto-coupler chosen was also a TI 4N49. The high sensitivity of the unit was unnecessary, but it was chosen to keep the variety of parts to a minimum. The circuit is trivial with a switch connecting the anode of the opto-coupler LED to V+ while the cathode is connected through a 1K ohm resistor to ground. From the data book, this circuit provides roughly 3.5 milliampere of current through the input LED. This will provide roughly 5 milliampere of current with less than .5 volt drop across the output photo-transistor. The output here is not well protected. Again overvoltage protection is offered since any damage will be stopped at the opto-isolator. But, connecting a 5 volt source across the collector and emitter terminals could destroy the opto-coupler by exceeding its power dissipation rating.

Memory Module

The memory module was designed to meet the following requirements:

1. Memory size greater than 64K by 16 bits
2. Module must be field replaceable to allow more storage
3. Low power consumption
4. Memory must be battery-backed with a thirty day minimum storage time.
5. Memory must automatically switch to internal batteries if data logger power fails
6. Memory must maintain data under all conditions

To meet these requirements a search was carried out for a STATIC RAM with low power consumption. After checking with several vendors, Hitachi HM4334P-4 memory chips were chosen. The units chosen have extremely low power consumption. The data sheet is shown in Appendix B. The chip is configured as 1K by 4 bits, and the pinout is a standard-memory chip pinout. The next step was to find a memory printed circuit board that used memory chips with the same pinout. After calling several manufacturers, only two were located that made such boards. A sample of each board was ordered and after receiving the boards, the schematic of

each was checked. As with almost all commercially available memory boards, both used low power schottky transistor transistor logic (LSTTL). Since one of the primary constraints is power, LSTTL is an unsuitable logic form. Replacing the LSTTL chips with a CMOS equivalent chip would decrease power consumption by 3 orders of magnitude. For both boards, only input, output and address buffering chips could be directly replaced. The address decoding circuitry could not be directly replaced.

At this point the final module design was completed. Each module would consist of eight memory boards (configured as 16K by 8 bits each) and two controller boards (which would handle the address decoding and some other functions). Additionally, one other board was added to these ten to accommodate easier wiring of the module. The controller boards, in addition to handling the address decoding, take care of power switching and data protection.

The memory is protected by gating the write pulse from the data logger. A flip-flop is reset if either the power fails, the top of memory is reached, or the user pushes the lock pushbutton switch on the front panel. The output of this flip-flop is used to gate the write pulse. The only means of setting this flip-flop is to push the front panel switches marked unlock (one for the lower half of the memory, one for the upper half). Pushing this

button will allow write pulses to alter the contents of memory. The condition of the flip-flop is indicated by the right and left hand decimal points in the memory pointer display. If a point is visible, then the respective part of memory is unlocked. If the point is not visible, then that portion of memory is locked. The logic level is important here. The flip-flop output to the data logger is a zero if the memory is locked. This is important since this is the condition of the flip-flop when the data logger is off, thus no current will flow to the data logger through the gate. See figure A-3 for the schematic.

The power switching function of the controller was initially designed as a relay circuit. Due to the high current consumption of relay coils, this idea was abandoned in favor of a solid state switching method. The circuit had only two requirements when the data logger is on. The voltage supplied to the memory must be at least 4.75 volts, and minimal or no current should be drawn from the battery. The initial design shown in figure 3 had the merits of simplicity, but could not supply the necessary voltage. Diode D2 will have about .6 volt dropped across it, leaving only 4.4 volts for the memory. Even using schottky barrier diodes, the best that can be done is about 4.7 volts. This is not really acceptable. Next the circuit shown in figure 4 was design and tested. In this circuit

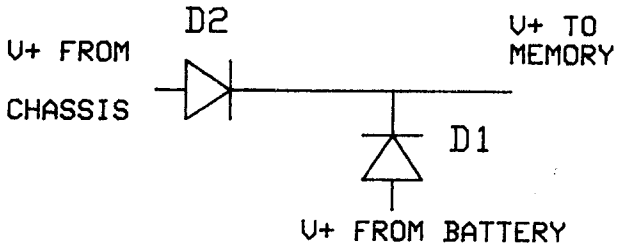


Figure 3. Initial Memory Power Switcher

D2 is replaced with a power transistor with a low collector emitter saturation voltage. R1 is chosen to saturate Q1 heavily. The circuit performs well until the data logger is turned off. The circuit can be modeled as shown in figure 5. In this case the memory powers the data logger (as was found experimentally). Again a new design was needed Finally, the circuit of figure 6 was designed. In this circuit, R1 and R2 are chosen such that Q2 is lightly saturated. R3 is chosen such that Q1 is heavily saturated. R4 is chosen experimentally. The circuit operates as follows. With the data logger on, Q2 is saturated, Q1 is saturated, and Q3 is cutoff. Thus the memory operates at roughly .1 volt below the data logger power supply voltage (5 volts). This is an acceptable value. When the data logger is turned off, Q3 becomes saturated and supplies current to Q2. This robs Q1 of base current which lowers the emitter voltage of Q1. As the emitter voltage of Q1 falls, Q2 eventually cuts off. This leaves Q1 and Q2 cutoff with Q3 saturated. With the circuit designed, the battery, B1, must be chosen.

The initial choice for B1 was a Nickel-Cadmium rechargeable battery. However the self-discharge rate of the Nickel-Cadmium type battery, renders it unacceptable. A typical Nickel-Cadmium type battery was at 60% capacity after 30 days. Several other rechargeable battery types were examined. All of which had their deficiencies. Next

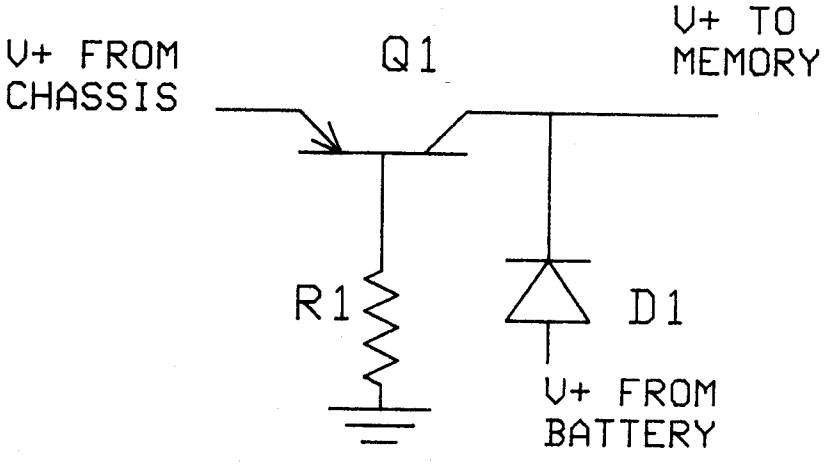


Figure 4. Revised Memory Power Switcher

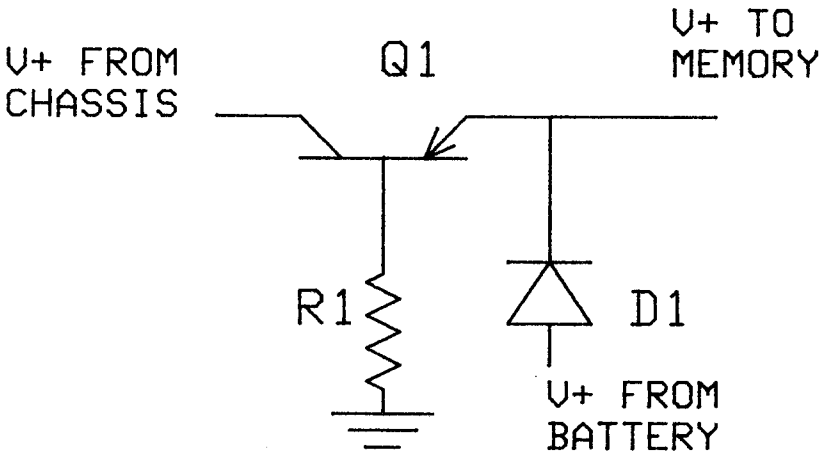


Figure 5. Model of Revised Switcher

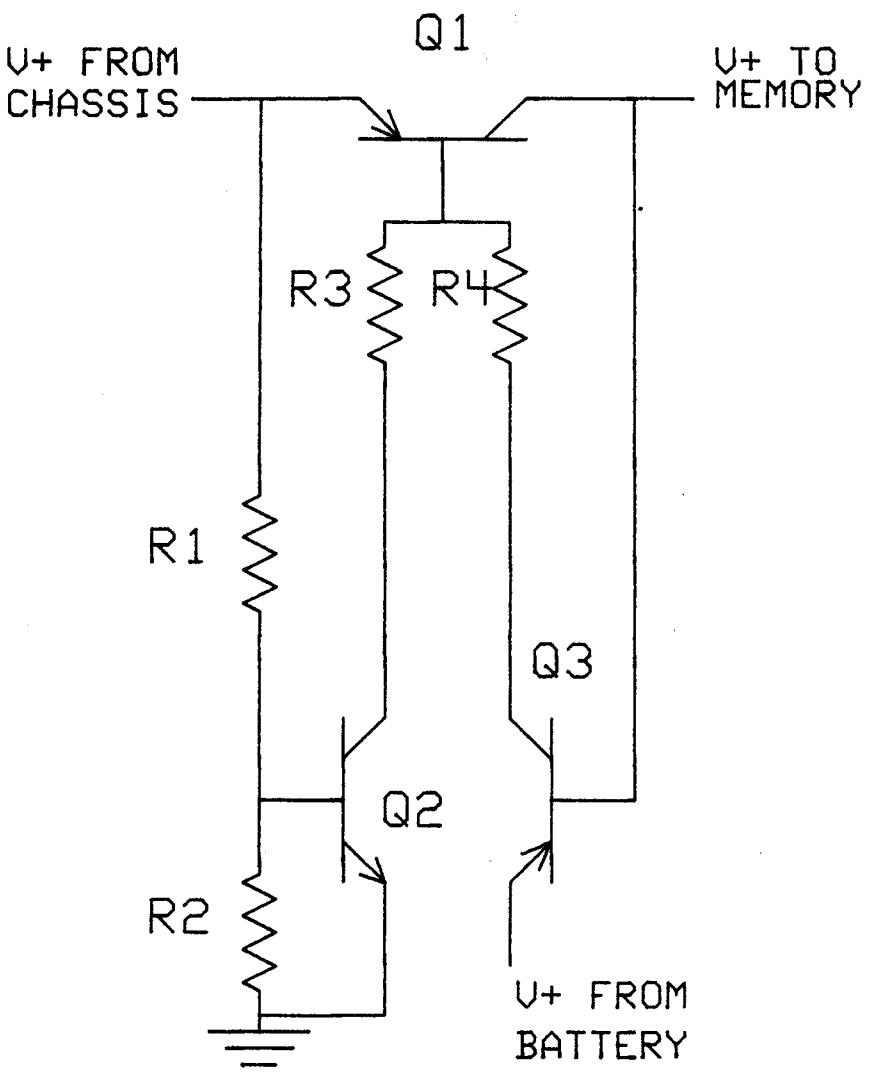


Figure 6. Final Memory Power Switcher

primary batteries were considered. Among these, the best were the mercury type batteries. This type exhibits a very long shelf life, has a flat discharge curve, and works well under light load conditions. The type chosen is also inexpensive and readily available. The type chosen is an E134N (discharge curve in appendix B). This particular battery has an initial voltage of 5.4 volts. The minimum voltage it must maintain to keep the memory intact is about 3.6 volts. This is computed from the minimum value necessary to keep the CMOS circuitry operational (3 volts) plus the base emitter drop in Q3 (about .6 volt under light loading). The battery was tested and the life was determined to be roughly 40 days. This met the design criterion.

Power Supplies

Since the input power is DC, DC to DC converters were required to obtain the required regulated voltages. In all cases, the regulated output needed to be isolated from the input supply. The data logger required $\pm$ 15VDC at approximately 50 milliampere, +5VDC up to 200 milliampere, and +5VDC at approximately 200 milliampere. The $\pm$ 15VDC supply was necessary for the data acquisition module. The +15VDC supply was also used to power the crystal oscillator in the time clock. The first 5 volt supply is necessary for all of the internal CMOS circuitry, memory, etc. The second +5 volt supply is used only when the computer

interface is active. The schematic is shown in figure A-15.

The supplies chosen are manufactured by Semiconductor Circuits Inc. The units were chosen for their low ripple noise at the output. The effeciency of a low noise output unit is not the highest but is still 55% to 70% effecient. The data sheet for the power supplies is shown in appendix B. A low noise output model was selected for the $\pm$ 15V supply to ensure power supply noise would not adversely affect the accuracy of the data acquisition module. For the +5V supplies, low noise is still important to reduce spurious signals in the digital circuitry.

The input to the power supplies contains a series power schottky barrier diode to prevent reverse voltages from damaging the power supplies. A schottky diode was chosen to minimize the voltage drop across the diode.

The mode switch does much of the power switching. In the XMIT mode, the switch activates the second +5 volt power supply which drives the computer interface circuitry. Normally this power supply is off to conserve power. The mode switch also de-activates a pair of EPROMS in the XMIT and LOG modes to conserve power.

Observation Counter

The observation counter module consists of two parts. The first is the counter itself and the second is the camera interface. The counter is presettable by simultaneously pushing the set switch and sliding the enable switch. This This operation sets the counter to the value selected via the thumbwheel switch directly below the counter. A double switch arrangement for setting the counter was selected to prevent accidentally disturbing the setting of the counter in the field.

The counter is very simple. It is the cascade connection of six presettable decade counters. The LSB counter up input is fed from the controller. This input is pulsed at the completion of an observation. Standard 74C series CMOS logic chips were used. Pullup resistors of 100K ohm were used for the thumbwheel switch outputs and the set input. The counters drive an LCD drive array, the camera interface, and a multiplexer input.

The camera interface is responsible for feeding the camera controller one BCD digit of the observation number at a time. The camera controller sends the data logger a 3-bit address which selects the digit desired. For example, an address of 000 base 2 would provide the least significant digit at the output of the camera interface. The input address-lines have zener-diode protection (Breakdown

voltage 5.6V) which provides additional protection against over voltage and reverse voltage transients. The full schematic is shown in figure A-4.

Physically, the observation counter is located on the third board behind the observation counter display. The camera interface board plugs into the observation counter. This board is the fourth board.

Controller

The controller was the most difficult circuit to design. The design uses a synchronous circuit with a four phase clock. The phases step the controller through various functions. Phase one is a control phase. Phase two writes the data to the memory. Phase three increments the memory pointer while phase four updates the address in the memory chips and executes some additional control functions. The idea of using a four phase clock was set down at the beginning of the design process. In the beginning of the design, a list of functions that the controller had to perform were listed. These included controlling the data acquisition module, the multiplexer, the memory address pointer, the observation counter, the time clock, and the memory module. After the functions of the controller were detailed, the design shown in figure A-5 was designed. The detailed description follows.

The data switch is debounced by a set-reset flip-flop composed of two NAND gates. (1/2 of IC8) 100K ohm pulldown resistors for the data switch were selected to minimize power consumption. The output of the flip-flop is OR'ed together with the external trigger signal. This signal is derived from inverting and buffering the external trigger input. Again a 100K ohm pullup resistor was selected to minimize power consumption. A 5.6 volt zener diode is also connected across the input to ground to protect the gate from under voltage and over voltage inputs. Additionally, the gate itself has some protection against voltage transients. (See appendix B device MM74C14) The OR'ed signal from the data switch flip-flop and the external trigger signal is OR'ed again (pin 8 IC10) with the output of switch S1. This signal will be referred to as the start signal. If S1 is connected to the clock input, then every two seconds the rising edge of this signal will trigger a one shot. (IC2 pin 1) If the switch is grounded, then the clock signal is disabled, and the one shot will be triggered by the data switch or a falling edge on the external trigger input. The start signal and the output of IC7 (pin 8) are NANDED together to drive the input of the one shot. The output of IC7 is high in the single mode of operation and is normally high in the repeat mode. It goes low only at the end of an observation when the controller is in the repeat mode. This will cause the logger to take the next observation at the completion of the first

observation if the start signal is held high.

Up to this point, all of the circuitry has been asynchronous. The one shot (IC2) is necessary to synchronize the start signal with the four phase clock. The method of synchronization is to set the one shot pulse duration longer than one full clock cycle. In this case, a 12 microsecond pulse length was selected. This insures that the flip-flop formed by 1/2 of IC20 is set on phase one through 1/4 of gate IC14 over the specified temperature range. When set, this flip-flop indicates that the logger is recording the header data, i. e. time, year, etc. When this flip-flop is set, the data acquisition module output is disabled and the digital multiplexer output is enabled. The clock module inhibit signal is also activated. See the section on the clock module for details of the inhibit signal.

The counter, IC21, will initially be set to zero. This counter controls which input of the digital multiplexer is selected. For example, if the counter output is 0001 base 2, then the day of the year passes through the multiplexer. The general sequence of events in recording the header data is as follows. On phase two of the clock, the digital multiplexer data as selected by the counter is written to the memory. On phase three, the memory counter is incremented and so is the multiplexer counter. On phase four, the updated memory address is stored in the memory

chips. This process continues until all of the header data is stored. After data is stored, the multiplexer counter will assume a value of 0110 base 2. When the counter reaches this value, several events occur. The LD ENB output to the data acquisition module falls low, setting the analog multiplexer to the first channel selected. It also triggers a one shot, IC3, which will start the initial conversion sequence. It sets the flip-flop formed by 1/2 of IC11. Finally, on phase four of the clock, it will reset the flip-flop formed by 1/2 of IC20. Resetting this flip-flop disables the digital multiplexer and enables the data acquisition system output. Thus the converted analog data can be stored. Resetting this flip-flop will also reset the multiplexer counter, IC21, on phase one for the next observation.

Triggering one shot IC3 causes the strobe input of the data acquisition module to go low. This starts the conversion of the first channel desired on the falling edge of the strobe input. LOAD ENABLE must be low during this falling edge to force the desired first channel into the analog multiplexer. The first channel to be converted is selected by the LAST/SINGLE switch. In the LAST position, the data logger will convert and store channels 1 through the channel selected by the channel select thumbwheel switch. If the switch is set in the single position, the logger will only convert and store only the

channel indicated by the thumbwheel switch. The function of selecting the first channel is executed with IC5. IC5 is a quad 2-input multiplexer which either selects a fixed input 0001 base 2 when pin 1 is high or selects the thumbwheel output when pin 1 is low. The The output of the multiplexer is fed to the analog multiplexer counter address input of the data acquisition module. The select input of the multiplexer is fed by 1/4 of AND gate IC7. The output will be high if LOG is high and switch S3 is in the LAST position. If switch S3 is in the single position or the logger is not in the LOG mode, then the multiplexer select line will be low and the first channel will be that selected by the thumbwheel switch. With this arrangement, if the logger is in the meter mode, then the only channel that will be converted is the desired one.

When the strobe input to the data acquisition module falls low, then the module begins the first conversion. At the completion of this conversion, the end of conversion signal (EOC) will fall low. This triggers one shot IC2. The pulse duration of IC2 is set for 12 microseconds. This is exactly one and one half full clock cycles. The circuitry following the one shot will function properly only if the pulse overlaps with either one or two pulses of the phase four clock signal. A pulse length of one and one half clock cycles will allow the greatest deviation of the pulse duration with time and temperature, while still

maintaining proper operation. Hence the selection of the 12 microsecond pulse duration.

The output of the one shot is then AND'ed together with the output of the IC11 flip-flop, in IC23. The IC11 flip-flop output will be high at this time as stated before. The output of IC23 drives the J-input of a J-K flip-flop. The Q output of this J-K flip-flop will be low. Hence the K-input will be low. On the next falling edge of the phase four clock, Q will go high. The next phase two clock pulse writes the converted analog data to the memory through AND gate IC23. This signal is NOR'ed together with the write signal from the header data part of the controller. The output is then inverted if the function switch is in the LOG mode. If the data logger were not in the LOG mode, then this output would always be low preventing data alterations of the memory.

On the following phase three of the clock, the memory pointer will be incremented through AND gate IC23. The output of this gate is combined with the increment signal from the header part of the controller in a similar manner to the write signal. Again if the unit is not in the LOG mode, the increment signal will not pass through the logic. This output is combined with the calculator increment signal from the calculator interface to form one of the final memory address increment signals.

On phase four of the clock, one of two possibilities occurs, depending on the last channel converted and the channel selected by the thumbwheel switch. If they are equal, then the A=B output of IC4, a four bit binary comparator, will be high and the output of IC20 will be low. This output will be referred to as the last channel converted signal. If this signal is high on phase four, then pin 11 of IC15 will also go high and pin 10 of IC11 will go low beginning the start of the conversion of the next analog channel. If the last channel signal were low, then the strobe signal to the data acquisition module would not occur. Instead, pin 3 of IC15 would go high. This is the end of scan signal (EOS). The EOS signal will, if the unit is in the LOG mode, increment the observation counter. In any mode, EOS will reset the IC11 flip-flop, and if the unit is in the repeat mode with the start signal high, start the next observation via IC7.

On the falling edge of the phase four clock, whether the J-input is low or high, the output of the J-K flip-flop will return low since the Q-output and the K-input will both be high.

Additionally, if the unit is in the meter mode, all of the circuitry functions identically, except the memory write pulse and memory pointer address increment pulse will be inhibited. The output of the channel indicated by the thumbwheel switch will still be available on the input

data bus to memory and the input of the display multiplexer.

The four phase clock generator is shown in figure A-6. The squarewave generator consists of a dual low power TTL one-shot. Each one-shot is set for a period of two microseconds. The one-shots are connected to guarantee self starting. Low power TTL one-shots were selected since a CMOS one-shot has very poor pulse length stability with such short pulses. The Q output of one of the monostables drives a J-K flip-flop that divides the frequency by two. The Q and Q inverse outputs of the divider and monostable are AND'ed together in the standard fashion to obtain a four phase clock. An OR gate was inserted into the Q inverse output of the monostable for a delay to eliminate a timing problem.

IC28 acts as a power on reset. The one-shot and the input buffer are powered from the time clock battery. With normal power applied, pin 6 of IC29 goes high which triggers one-shot IC28. The outputs of this one-shot are buffered through IC24 to generate the reset and reset inverse signals. These signals force the controller into a known start up state. The buffers selected here are MM74C902. These buffers allow voltages above their own VCC level. Thus even when IC24 is not powered, it is not damaged or draw excessive current from IC28.

The flip-flop formed by IC8 serves no purpose. It was installed and later found to be unnecessary. It was never removed. The repeat/single jumper is located on the controller board and is usually set to single for field work. The external trigger input is designed to accept a simple switch input. However, in reality, it is not recommended since most switches bounce and this could cause errors or multiple observations. A TTL, CMOS, or NPN transistor switch is recommended. Finally, the channel select switch uses 100K ohm pulldown resistors which are not shown in the schematic.

Computer Interface

The computer interface was designed to interface with a PDP 11/34 computer with a DR-11C 16-bit parallel interface. The initial goals of the interface were isolation of the computer and data logger and moderate speed performance. In the later models, isolation will be reduced.

In the prototype, the interface consists of a buffer from memory, opto-isolation, output buffer, and control logic. The output buffer, some of the control logic, and the opto-isolators require a separate power supply to maintain complete isolation. This extra supply is active only when the data logger is in the XMIT mode to conserve power. The buffers from the memory have tri-state outputs, which are in the high impedance state except when the data

logger is in the XMIT mode. Thus almost all of the circuitry for the computer interface (see figure A-7) is either disabled or off when unnecessary.

When the function switch is first switched to the XMIT mode, several things happen. The memory buffers (IC16, 17,and 18) become active. Power to the optocouplers (IC6 through 14), the output buffers (IC1, 2, and 3), and the TTL control circuitry is applied. Finally,the rise on the XMIT line causes a one shot (IC20B) to be triggered. This one shot has a relatively long time constant (approximately 500 milliseconds) to insure that the flip-flop formed by IC5A and IC5B is set, i.e. the data valid signal is high.

The DR-11C interface operation is very straightforward. When the NEW DATA READY signal is asserted, the interface assumes the data on the input lines is stable. The data will then be transferred to the computer during the next positive pulse of the DATA TRANSFERRED output of the DR-11C. This pulse is approximately 400 nanoseconds in duration. For the complete description of the DR-11C interface, see appendix C.

The data logger's computer interface was designed to interface with the DR-11C. The interface is flexible enough to operate with other computer interfaces as well. The operation of the interface under normal conditions is

as follows. The DATA VALID output is normally high. This indicates the contents of the current memory location are available at the output. After the computer indicates it has transferred the data (REQUEST NEW DATA input goes low), one shot IC4 is triggered. This resets the IC5A and IC5B flip-flop which brings the DATA VALID line low. The one shot also transmits a pulse that is approximately 25 microseconds long through opto-coupler IC15. This pulse at the output of the opto-coupler is a negative going pulse. This pulse is passed through gate IC21C. The output of IC21C feeds another gate, IC21D. the pulse through IC21D increments the memory pointer. The counter is incremented on the falling edge of the pulse. The output of IC21C also drives the input of one shot IC20B. This one shot is triggered on the falling edge of the pulse. The one shot is responsible for generating the return pulse of approximately 25 microseconds. The return pulse passes through opto-coupler IC14 and sets the the flip-flop formed by IC5A and IC5B. The DATA VALID signal will not return high until the reset input from the output of IC4 returns low.

The input from the computer is protected by D1 and D2. These diodes prevent under voltage and over voltage inputs. R41 and R40 are used to improve the noise immunity of the interface. IC3F is a schmidt trigger type inverter, which also improves the interface's performance against noisy inputs. LED-1 is used as a status indicator. If the

LED glows, the interface is ready. If the LED is not glowing, then the interface must be reset before it will operate. The interface can be reset by switching the function switch to any mode and then back to XMIT mode. During data transfer, the LED should not extinguish. If it does, it indicates data is being requested (i. e. REQUEST NEW DATA pulses) before DATA VALID returns high. As a general rule, the interface can handle up to data rates of 10Kwords per second.

The opto-isolators chosen were 6N139s' and HPCL-2731.(dual 6N139) The data sheets for both devices are shown in appendix B. These opto-couplers were chosen since they are CMOS/TTL compatible. The input LED resistors were set at 1K ohm. With this value resistor, the current of the input LED is approximately 1 milliampere. The output pullup resistors are 5K ohm. A 5K ohm resistor is sufficient to guarantee a TTL only 1 milliampere of current to the photo-transistor when it is conducting. Thus the photo-transistor will sink an additional 7 milliampere of current and still maintain a TTL '0'. This is more than enough current to drive the single TTL gate at the output of the opto-coupler.

The 25 microsecond time constant of the one shot IC4 was chosen to allow for the memory counter to be incremented and stabilize, (2 microseconds maximum) time for the memory chips internal registers to be updated, (8

microseconds maximum or one full clock cycle) and time for this new data to stabilize at the output of the interface. (about 4 microseconds) The total estimated time required is 14 microseconds. Additionally, a wide safety margin was desired to insure error free data transfer. Hence the pulse length was increased to almost twice the necessary time. One shot IC20A must also be set to 25 microseconds to match IC4's pulse length. The pulse length of these two one shots must match to insure that the flip-flop formed by IC5A and IC5B is set. This will be guaranteed even if both one shots have the same duration since the return path is delayed by two opto-isolators. These opto-isolators provide a delay of roughly 2 microseconds each for a total of 4 microseconds. The flip-flop is designed so that even though both inputs are asserted, the DATA VALID output is low. This is a requirement because this is a common occurrence in this design.

After the interface was initially connected to the computer, additional work was necessary. C11 was added to slow down the output of opto-coupler IC15. This capacitor eliminated all but a few of the multiple pulses to the memory pointer. Before this capacitor was installed, the computer might request 100 data words, but the memory pointer would indicate anywhere from 150 to 200 words had been transferred. Even with the capacitor, a computer request of 100 words would result in 101 or 102 words

transferred according to the data logger's address pointer. The solution to the problem was not obvious. By connecting the ground of the isolated interface to the chassis of the computer, the problem was completely eliminated. To date, with the above grounding arrangement, over one hundred thousand data words have been transferred without error.

BCD Display Drivers

Since the displays that were selected for the front panel were liquid crystal displays (LCD), suitable decoding and driving circuitry was necessary. The decoding circuitry is standard BCD to seven segment decoding. To drive the LCD it is necessary to apply a squarewave (0 to 5 volts) at approximately 60 Hz to the backplane. To make a segment of the LCD visible, a signal 180 degrees out of phase with the backplane is applied to that segment input. A segment will not be visible if the segment input is floating or if the signal is in phase with the backplane. The only chip capable of both decoding the BCD digit and driving the LCD was a CD4543BCN. (see appendix B for data sheet) Each chip is capable of driving one digit in the display. Hence six are required for each display. There are three such displays necessary, the time, observation number, and data displays. The schematic is shown in figure A-8. The data display has a small capacitor, .001 microfarad, from ground to the right colon segment to make it visible all of the time. This is a simple method to force a segment on since the segment will be excited by an ac signal without a dc offset, the basic requirement to drive an LCD.

Digital Multiplexer

The digital multiplexer selects the digital data that is to be written into the memory module through the input data bus. The multiplexer is formed from an array of quad 2-input multiplexers. There is a three levels of multiplexing required with this scheme. After the multiplexers, there is a tri-state bus driver which puts the data onto the bus. These drivers are active only at the beginning of an observation. Most of the time they are in the high impedance state. The schematic of the multiplexer is shown in figure A-2.

The control inputs to the multiplexer are from the control circuitry. PM-1 is the least significant bit of the control counter, PM-2 is the next significant bit and PM-3 is the following bit. PM-4 is the multiplexer disable input. A high input on PM-4 disables the output of the multiplexer. The various inputs to the multiplexer are described above the input. All inputs consist of three BCD digits, except the start code which is 1010 base 2.

A control input of 000 base 2 will select the input the data coming through connector JM-7, an input of 001 base 2 will select the data coming through connector JM-6 and so on. Inputs greater than 101 base 2 will not be generated and used under normal conditions, so no provisions were taken to handle these signals in a systematic way.

Memory Pointer

The memory pointer consists of a set of four 4-bit counters. The use of binary counters as opposed to BCD counters simplified the memory pointer decoding. It was felt the additional circuitry required to allow the user to set and read the memory pointer in BCD was not worthwhile. The schematic is shown in figures A-9 and A-10.

The counters are set via the thumbwheel switches located below the address counter display. Once these switches are set to the desired location, the ENABLE switch is activated and the SET switch is depressed. The counters will then change to the new address. Two inputs to the counters are provided through NOR gate IC5. NOR gate IC5 also provides a complemented version of the most significant bit of the address to the memory module. Additionally, one shot IC5 provides a pulse of roughly 10 microseconds when the memory address wraps around from FFFF base 16 to 0000 base 16. When this happens, the memory module would protect itself so that no earlier data would be destroyed. Shown also in the schematic are the lock and unlock switches for the memory module.

The display for the memory pointer posed a new problem. The display decoder drivers used for the other displays will not operate for non-BCD data. In fact,

there is no IC available that will decode a hexadecimal input into a seven segment display code and drive an LCD. Therefore, the two functions were separated. The decoding of the hexadecimal input into seven segment code was handled by an MC14495BC. (see appendix B for data sheet) This chip then drives eight exclusive-OR gates with their second input being driven from a 60 Hz squarewave derived from the clock module. Spare exclusive-OR gates gates drive the memory lock status indicators, (the two decimal points) and the radiometer battery indicator. (the colon) The exclusive-OR gates provide the required signals to drive the LCD properly. Physically, the LCD is mounted on the first board, the exclusive-OR gates are located on boards 1 and 2. The decoder and counters are mounted on boards three and four.

Display/Calculator Interface

The display/calculator board is responsible for providing the interface to the HP-97S calculator, to allow proper display of any valid type of data stored in the memory, and to display the data from the data acquisition module when desired. It's main function is to display the data to the front panel. The schematic is shown in figure A-11.

The calculator interface is very simple. When the calculator's DATA REQUEST output falls low, this triggers

a one shot, one half of IC7. The Q output of this one shot rises high which increments the memory pointer. The one shot has a pulse duration of 25 microseconds. This pulse length allows ample time for the data to settle on the output lines to the interface. On the falling edge of the Q output, another one shot is triggered, the other half of IC7. This signal, when high, loads the calculator interface with the data. Additionally, the selection of the start code was influenced by the HP-97S. By selecting a code of 1010 base 2, the interface would interpret the start code as a decimal point. Thus it is very simple to find the beginning of an observation with the calculator. This start code will also blank the LCD digit, so that the operator can easily find the beginning of an observation in the data logger. The HP-97S interface is very flexible and too detailed to discuss fully. For a complete description, consult the owners manual.

The decoding circuitry must be able to interpret two types of data. The first type is the header data. In this case, the data should be passed as four BCD digits to the calculator interface and display decoders. The other type of data is the converted analog data. This data word can be broken into two pieces. The first piece, the lower four bits, is the analog channel number. The second piece is the analog channel data. This is a 12-bit binary representation of the analog data.

The decoding of the lower four bits was accomplished with a four bit adder and some additional logic. The four lower bits are decoded into their equivalent two BCD digit representation. Decoding in this manner will be correct in both the case of of the BCD header data, which is always 0000 base 2 or 00 base 10, and analog channel data which will be between 0001 base 2 to 1111 base 2 or equivalently 01 base 10 to 15 base 10. The method of decoding is to first, with combinational logic, determine if the lower four bits are greater than a BCD '9'. If they are, then a BCD '6' is added to the input data. In binary arithmetic, binary 1010 plus binary 0110 is a BCD '0' plus carry. Similarly, the decoding scheme works for any other four bit binary number greater than 1010 base 2. If the input number is less than 1010 base 2, then nothing is added to the input and it passes through the adder unchanged. Therefore, the decoding works properly for all possible inputs.

The upper 12 bits of data cannot be decoded as easily as the lower four bits. The 12 bits pass through the board unchanged if the data logger is in any mode except LOG/DISPLAY or METER modes. If the logger is in one of these two modes, EPROMS IC8 and IC9 will be powered up. If the lower four bits are 0000 base 2, then again the upper 12 bits will be passed through unchanged to form the lower three digits to the left of the colon on the data display.

The most significant digit on the data display will be blanked since R1 through R4 will pull these lines high. If the calculator interface reads this BCD digit, it will be interpreted as a NO-OPERATION command. If the lower four bits are not 0000 base 2, then the upper 12 bits will be decoded into their four digit BCD representation by the EPROM's, IC8 and IC9. IC5 and IC6 will be in the high impedance state and IC15, IC16, and IC17 will be active to transfer the decoded input to the display and calculator connector.

The multiplexers, IC1 through IC4, perform two functions. First, they select the data that will be decoded. If the logger is in the meter mode, then the output from the data acquisition module will be selected. In all other modes, the output from the memory module will be selected.

The second function of the multiplexers is that of protection. If the EPROM's are not powered, then all of the address lines should float or be low to prevent damage to them. In this case, a low input was easy to generate by taking the enable signal on the multiplexers high. This forces all of the multiplexer outputs low. It was not necessary to disable the multiplexer for the lowest four bits since this multiplexer drives only CMOS gates which are always active. IC5 and IC6 take their inputs directly from the memory module output directly. Therefore, even when the multiplexer is deactivated, the 12 bits will

still pass through to the data display allowing the proper display of the header data.

The idea of using EPROM's to do the data decoding came mainly from the simplicity of the implementation. The only other alternatives were a microprocessor or some sort of dual counter technique. The dual counter would be a very good approach with respect to power, but would add considerable control circuitry, and would be very slow, approximately 8 milliseconds worst case. The basic idea is to pulse a decade counter and a binary counter together. When the binary counter reaches the input value, the decade counter would reach the proper BCD representation of the input. The long conversion time and additional control required eliminated this scheme. The microprocessor approach would save little or no power and would be more complex. Hence the EPROM approach was selected. To conserve power, the EPROM's are not powered when they are not in use. The EPROM's when powered consume approximately 130 milliamperes from the +12 volt input source.

Time Clock

The time clock had several requirements. First, it had to provide the necessary 60 Hz squarewave to all of the other LCD drive circuits. It had to switch to internal battery power whenever the data logger is off. The batteries must be able to keep the clock running for 30 days.

Finally it had to interface to the digital multiplexer.

The generation of the 60Hz squarewave was executed with a crystal oscillator and divider IC. See figure A-12 for schematic. This IC requires a power supply of at least 7 volts, so it is powered by the +15 volt power supply. The 60 Hz squarewave output of IC7 must be buffered to prevent damage to the gates that follow it. IC4 is powered by the +5 volt power supply only, and will protect the other front panel modules from damage even if the clock is powered and the data is off. The IC5 buffer is necessary only for the voltage translation of the squarewave from IC7 from 0 to 15 volts to the desired 0 to 5 volt swing. The output of this buffer drives a delay flip-flop, whose function will be described later, and the clock counters. The clock consists of three divide by 60 counters and one divide by 24 counter. The first counter, divides the 60 Hz signal down to 6 Hz. IC4A in conjunction with some other gates divides the 6 Hz signal down to 1 Hz.

The operation of the divide by six counter is roughly the same for all three units. When the counter reaches a value of five, the output of the respective NAND gate falls low. This brings the clock input on the following counter low as well. When the counter reaches six, the AND gate brings the RESET input of the counter high which resets the counter to zero. The output of the NAND gate

also goes high which increments the following counter by one as desired. The output of the divide by ten counters is taken from Q4. When the counter cycles from nine back to zero, Q4 will fall low. By connecting Q4 to the input of the following counters ENABLE input, this falling edge will increment the following counter at the proper time.

The 1 Hz, from IC4A, is gated through an AND gate to allow stopping the clock to set the time. IC3B is the seconds counter and IC3A is the tens seconds counter. 1/60'th of a Hz output from IC3A is gated through an exclusive-OR gate. The other input to the exclusive-OR is grounded unless S2 is depressed. If S2 is depressed, then the minutes input will be clocked at a 1Hz rate instead of the normal rate for setting the minutes and tens minutes counters. IC2B is the minutes counter and IC2A is the tens minutes counter. The one pulse per hour output of the tens minutes section is gated through an exclusive-OR in the same manner as the tens tens second output to proved a set switch for the hour counters. In the case of the hours counters, these must be reset when their count reaches '24', for a 24 hour format clock. The reset is obtained by AND'ing the Q2 output of IC1A, the tens hour counter, with the Q3 output of IC1B, the hours counter, and feeding the gates output to the reset inputs for both counters.

The last requirement of the time clock is to interface with the digital multiplexer. The first requirement

for the interface to the multiplexer is to disable the outputs when the power to the data logger is off to protect the circuitry in the multiplexer. This function is handled by disabling IC1 through IC3 on board two of the time clock. The output of gate IC5 will go high when the data logger is off. This will force the disable signal on IC1 through IC3 high, de-activating their outputs. The second requirement for the interface is that it must provide a valid time output. Because of the relatively long time it takes for the counters to change states, circuitry must be designed to latch the time data when it is valid. A very rough estimate of the maximum propagation time from the seconds counter input to the hour counter stabilizing could be obtained by taking 650 nanoseconds, the maximum propagation delay time of the counters used, times six counters to obtain roughly 4 microseconds. Hence it would be possible to send the multiplexer an invalid time if some sort of latching of the time data did not occur. The scheme used could have one of three possible alternatives. The first and simplest is if the clock inhibit signal rises high, indicating the multiplexer will be querying for the time in about 16 microseconds, and there is no positive pulse transition on the 60 Hz input to the clock counters. In this case, the Q inverse signal of the delay flip-flop IC6 will remain high. This implies the LATCH ENABLE on IC1 through IC3 will remain high which allows the counter outputs to pass through the latches giving the

correct time to the multiplexer. The second possibility is for the clock inhibit signal to rise high, indicating the multiplexer will be reading data shortly, and then a positive pulse occurs on the 60 Hz input to the clock counters. Using maximum propagation times, 300 nanoseconds later, the latch enable input will fall low, which will cause the latches to retain their current data. Using average propagation delay times for the counters, 325 nanoseconds each, it will take at least 650 nanoseconds for the seconds counter to be pulsed. It would be even longer when the delay time through the two NAND gates in the path are considered. This gives a two-to-three safety margin on latching the data before the first counter changes. The third and last possibility is the case of a positive going pulse on the 60 Hz input to the clock counters just prior to to the clock inhibit rise. In this case, the latches will not latch the data. Within 6 microseconds (8 times 650 nanoseconds instead of 6 times) all counters will again be stable, and only after 16 microseconds will the data be read by the multiplexer. In this case the safety margin is even greater, almost three-to-one.

Front Panel Circuits

Figure A-13 shows the remaining miscellaneous circuitry in the data logger. In the upper left hand corner of the figure is the power switching for the EPROM's and the

generation of the LOG, METER, and XMIT signals. In the center of the figure are the other multiplexer inputs. The START code can be rewired internally to obtain a different code if desired. The YEAR thumbwheel switch, as well as the DAY OF YEAR thumbwheel switch use thin film resistor arrays for pulldown. Each resistor in the array is 100K ohms. Finally, the pushbutton switch array that selects the observation code is also shown. Each switch is a DPDT switch that sets either one or two of the four bits set aside for this information. The status switch has an output for the radiometer interface and the multiplexer.

A/D Converter

The A/D converter that was selected is a complete data acquisition system. The unit contains a 16 channel analog multiplexer, amplifier, sample and hold, and a 12-bit analog-to-digital converter. There is also a small amount of control circuitry in the module. The converter chosen is a DM6812 which is manufactured by Analogic Inc. The data sheet for the unit is shown in appendix B. The 'DM' version of the 6812 was chosen for its improved specifications and its availability.

The unit is configured for single-ended operation by connecting pins 19T to 17B, 18T to 18B, and 12B to ground. See figure A-14 for details. Analog channel 0 is unused and is tied to ground. Any other unused inputs should also

be grounded. Full 12-bit resolution of the converter is desired so pin 28T, the short cycle pin, is grounded. The CLEAR ENABLE is not used, and is grounded. A normal input voltage range of zero to five volts was desired. To obtain this scale, pin 13B is tied to pin 12T, and 13T is connected to 14B. This scale can be changed to zero-to-ten volts by changing the soldered jumper from 13B to 12B. The analog channel returns are not tied together or to ground until very close to the Analogic module.

The internal delay, to allow for settling of the analog multiplexer and sample and hold circuits, was utilized by connecting 23T to 26T. The output coding scheme is straight binary, i. e. 000 base 16 is zero input and FFF base 16 is full scale. The coding is set by connecting 23B to 24T. The control inputs and outputs are described in the section on the control circuitry. The A/D tri-state enable signal to the board controls IC1 and the tri-state output of the A/D converter. When low, the A/D converter outputs are active, putting the 12-bit converted signal on the upper 12 bits of the bus, and the analog channel multiplexer counter data passes through IC1 to the lower 4 bits of the input bus to memory. When the enable signal is high, indicating header data is being stored, the A/D converter outputs go into the high impedance state, and the four outputs of IC1 will all go low. Thus the lower 4 bits will be zero, indicating header data.

DATA LOGGER CONSTRUCTION

Mechanical Layout

The actual design of the chassis and memory module was completed by Barrett Robinson. The front panel layout was a mixture of what was desired and what was possible due to construction constraints. The actual size of the data logger is 9.8 x 12.6 x 18.9 inches. The plug in memory module is 8.3 x 6.7 x 12.0 inches. The main chassis is 9 Kg. while the memory is 2.7 Kg. Various views of the chassis are shown in figures A-16 through A-21.

Board Construction

The printed circuit (PC) boards for the data logger were designed and the artwork prepared at LARS. The actual PC boards were manufactured by a commercial vendor. The approach taken was to build a board for each functional block. In some cases functions were combined onto a single board. Refer to the schematics for the details of the location of a circuit. Shown in appendix A is the part and jumper locations on each board. Also in appendix A are the parts lists. The controller board was constructed on a

proto-typing board as opposed to a custom PC board to allow changes if necessary. The actual board layouts were very straightforward, but time consuming. Bypass capacitors were used on the boards, but these are not as critical as with TTL due to the much lower power consumption. Boards were connected via berg type ribbon cable assemblies. This was later found to be a messy and inefficient means of making electrical connections. In addition to the berg type jumpers, there were several single wire board to board and board to external connector jumpers.

Shielding

The analog signals were shielded by carrying the signals from the connector to the A/D board over a short piece of ribbon cable. The ribbon cable had alternate return and signal lines to prevent interchannel crosstalk in the cable. The Analogic module has RF and EMI shielding on all six sides. Located underneath the module is a ground plane for additional shielding. The chassis case is connected to analog ground which will provide some shielding even though the chassis is made of aluminum as opposed to steel. The analog signal wires are connected close to the Analogic module so that the distance the signals must pass over is minimized on the PC board.

Connectors And Cables

The connector chosen to interface the memory module to the main chassis of the data logger were a pair of Amphenol Blue Ribbon connectors. Each connector has 32 contacts for a total of 64 possible connections. Of the 64 possible, 60 were utilized. The amphenol connector was chosen for its ruggedness and floating female connector. The floating female connector allows for some misalignment without preventing or degrading connector mating. The connector chosen for the computer interface is a standard 25 pin Delta connector. This was chosen for its almost universal use as a computer interface connector. This type of connector offers a high density of contacts per unit area. The external trigger connector is a BNC type. This type was chosen for its wide use and its locking feature. That is, once the matching connector mates, the connectors will not separate by accident.

The cable chosen for connecting the radiometer to the data logger has a shielded twisted pair for each signal. The shields are connected to ground. The twisted pairs are a pseudo-differential source arrangement to prevent ground loop problems. This type of cable offers very high immunity to stray fields. The power cable runs beside the signal cable. This cable consists of a twisted shielded pair. The 12 volt power and return lines are shielded with ground. The camera cable selected is the same type of

cable with fewer conductors. Again, its selection was based upon shielding.

Control Function Philosophy

The front panel layout and control philosophy is on of the main reasons LARS was interested in building a data logger. Most of the data loggers on the market require several days to understand how to program and use them. We were interested in designing a front panel and control scheme that an untrained non-tehnically oriented user could learn to operate in just an hour or so. To carry out this concept, several key ideas were implemented. Full display of all pertinent data at all times is one. Thumbwheel switches with separate set buttons also are important. A large data button with a separate code button for each type of data to be collected. In the case of field use, the user will probably only utilize the CAL button for tagging a measurement from a standard, the DARK button for tagging a measurement of no signal, and the STATUS button to record the gain values of the radiometer channels. Field HOT and COLD blackbodies may also be available for calibrating the thermal channel. The RAD button would be depressed to indicate a measurement of a radiance standard and similarly the IRR button would be depressed to indicate measurement of an irradiance standard. Both of these standards are usually only available in the laboratory. They were included for completeness.

The philosophy of designing an easy-to-use instrument has its drawbacks. The data logger is not as flexible as many of the loggers on the market. It is much faster in recording the data and is easier to use however. The front control panel is also larger, due to the extra switches required. Marking the switches clearly is also important. Again, this requires more panel space, but is justified in better understanding of the controls without a manual. The connectors chosen were carefully selected. None of the external connectors to the logger are alike. Thus it is impossible to plug a cable into the wrong socket. All of the connectors are mounted on one side of the logger for convenience. Finally, all of the connectors that will be used in the field are either Bendix connectors or a connector that can be held in place by a latching mechanism. This is important to prevent accidental disconnection of a cable in the field. Bendix type connectors not only offer latching, but are very reliable in field conditions because of their tight sealing. Unused connectors are capped to further enhance their seal against dust.

PERFORMANCE TESTS

Time Clock

The time clock was powered from internal batteries for a thirty day period. The initial time was set according to WWV. At the end of the thirty day period, the clock was within ten seconds of WWV of WWV time. This easily met the thirty second specification set previously.

General Temperature Tests

The data logger was tested in an environmental chamber at 0, 25 and 50 degrees centigrade. The unit was checked for proper operation in the METER, LOG, and LOG/DISPLAY modes. It was not possible nor felt necessary to test the XMIT mode over temperature. All functions operated properly. At the low temperature extremes, the liquid crystal displays responded much more slowly to change. It took roughly one half second for the new digit to appear in the display. It was not possible to test the calculator interface due to the size limitations of the chamber. Since the data display operated correctly, the calculator interface should function over the 0 to 50

degree range assuming the calculator functions properly.

Analog Data Temperature Test

During the general temperature test, analog channel inputs one through fourteen were tested for temperature drift. Channel fifteen was not tested due to an oversight. See figure 7 for the test setup. The test involved measuring the two reference voltages and ground twenty times with the data logger at the three temperatures. The reference was measured with a Fluke model 8100A four and one half digit DVM. (serial number 4174) At the highest temperature range, with the 4.746 volt reference, all channels, all samples measured 3901 counts. At 25 degrees, same reference voltage, all channels, all samples were either 3900 or 3901 counts. At 0 degrees, all channels, all samples 3901 counts. Similarly, for the 2.231 volt reference, over the three temperatures tested, all channels, all samples were either 1843 or 1844 counts. With zero volt input, i. e. inputs grounded, all channels, all samples measured either 15 or 16 counts. This is within the ± 1 bit specification of the Analogic module and our specification.

Linearity Test

The linearity of the system was measured by applying a DC voltage to the input of all 15 analog channels and measuring the DC voltage with a four and three quarters

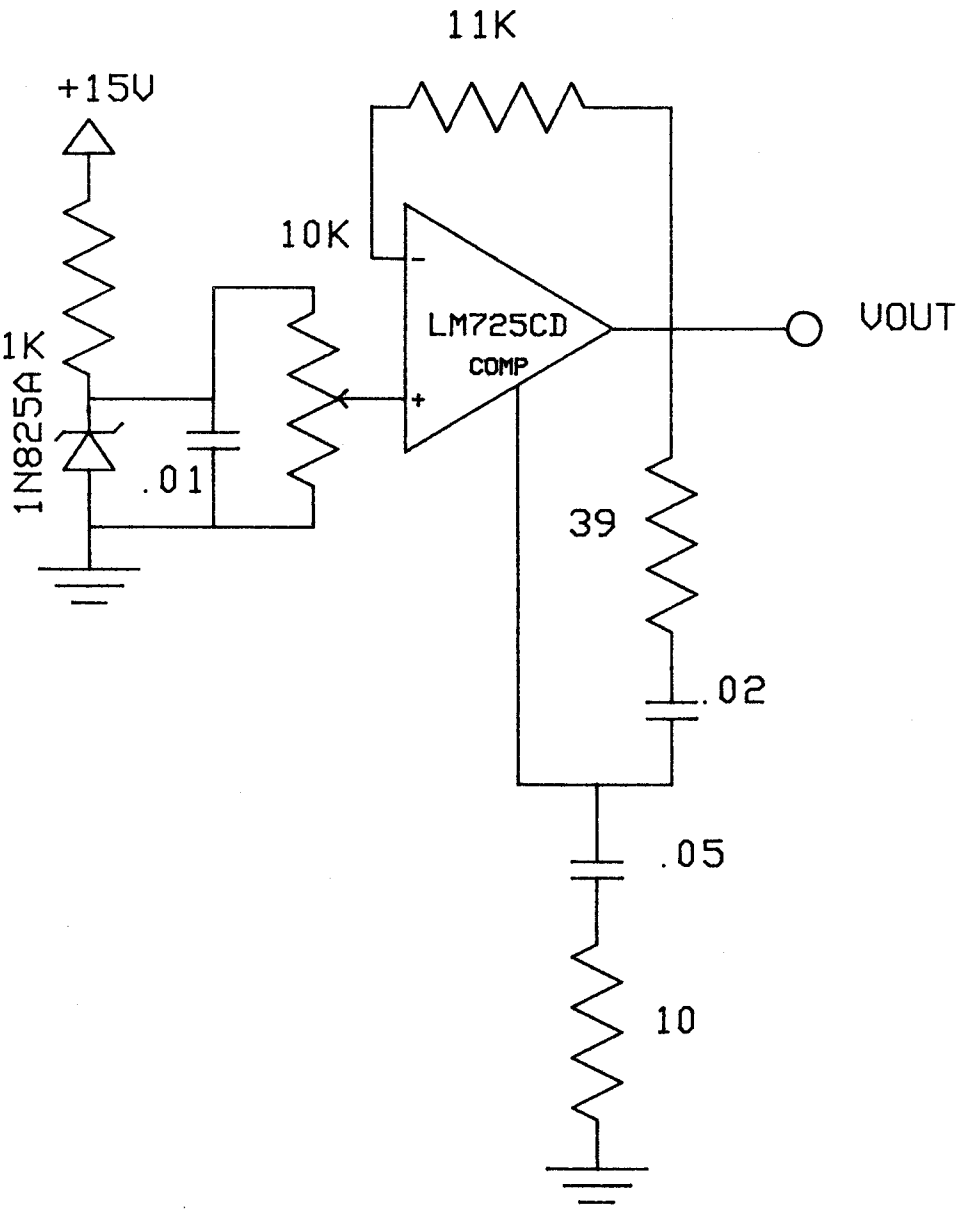


Figure 7. Precision DC Source

digit Fluke data logger. Over input voltages over the range zero to four volts, the Fluke logger was set on its four volt range. Above four volts, the Fluke was switched to the forty volt range. On the forty volt range, 27 voltage points were sampled 5 times each, on both the reference measurement logger and the logger under test. On the four volt range, 81 voltage points were sampled 5 times each. The 5 values were then averaged in both cases for a single data point. Separate least squares curve fits on the four and forty volt data were performed. The results showed the standard error of estimate for the forty volt range is at worst 1.6 bits. For the zero to four volt range data, the standard error of estimate is less than one bit. It was felt that the second error estimate is more accurate since measurement error in the reference voltage will contribute to the error estimate for the forty volt range data. More accurate measuring equipment was not available to perform more accurate measurements above four volts. The voltage reference utilized in this test is the same as the reference used in the environmental tests. The variable resistor was adjusted to produce the various voltages required.

Other A/D Tests

Two other tests were performed on the analog section of the data logger. The first is the DC drift performance of all 15 analog channels over time Over the entire use

period of the data logger, approximately five months, with either a 600 ohm source impedance or short from channel ground to input, the converted value has been within one count of 16. Thus the offset drift with time is negligible. Gain errors with time have not been checked. The final test is crosstalk performance. Alternate channel inputs were grounded through a 600 ohm resistor. The remaining inputs were excited by a zero to five volt sine wave at 1 KHz. Several hundred observations were recorded. In no case did the interfering channel cause an error of more than one bit on the grounded inputs. Additional test on the analog system were not performed. The converter met all published specification that were checked and it was felt it would meet all of the specifications if checked. See appendix A for the complete set of specifications for the Analogic module.

Memory Module Tests

The two basic tests performed on the memory included reliability of the memory with time and any problems associated with switching power to and from the internal batteries to the data logger power. The reliability of the power switching was tested by switching the data logger on and off five times at approximately 30 second intervals. The contents of 21 memory locations were examined before and after the test. This was repeated two more times. In no case was the data modified by repeated power switching.

In each case, the memory protected itself. In addition, the memory module was disconnected from the data logger to check for data loss. Again, the data remained intact and the memory protected itself. This test was performed with the logger powered and unpowered three times on 21 data locations.

The second test was over approximately a fifteen day interval. The unit was loaded with 42 data words. After the interval, the memory was interrogated for the data. The data was still valid. Along these same lines, the battery life was checked. Data was loaded into the memory, and each day was checked for correctness. The data remained valid for just over two months. After that period, data would not be held with the unit off. Since only 50 percent of the memory chips that the battery was powering were installed, the life of the battery must be interpolated to half of the measured life. This still meets the 30 day minimum battery life requirement.

With the exception of one memory board, all functioned properly when first installed. The one board had a sliver shorting two traces together. With the sliver removed, that board functions properly too.

The above tests do not exercise the memory as well as it should. In addition to these tests, another test was performed every time analog data testing was performed via

the computer. All of the programs written to analyze the analog data checked the digital data for correctness. All of the digital header data stored with each observation is normally known. The exception is the time. In most cases the time could be checked, but occasionally it was not. Any errors in the data recording, storage, or transfer of the digital data could be easily checked. No errors were discovered. Several thousand data points were tested in this manner offering a larger data sample that verified the proper operation of the memory module.

Other Tests

The final test was rudimentary vibration testing. Field environment vibrations were crudely simulated by dropping the instrument from a one inch height onto a hard surface while collecting data at 100 samples per second. The input voltage was approximately 2 volts. No errors in operation were produced. Similarly, lateral wraps on the instrument causing movements of two to six inches were performed under the same conditions. Again no errors were observed.

The data logger failed the most violent vibrational tests. On two airline flights, baggage handling caused some of the front PC boards that drive the LCD's to come loose from their connector. Additional support will be added to these boards. Other than this slight damage, the

data logger even passed this severe test, except for the partial destruction of the external trigger connector which was repaired easily.

SUMMARY

Performance Review

A data logger was designed and built with a 12 bit A/D converter offering complete observation consisting of the digital header data and fifteen analog channel values in less than 800 microseconds. Speed performance improves when fewer analog channel values are converted and stored. The data logger will interface with several devices including a PDP-11/34 computer, HP-97S calculator, HP-85 computer, LARS model 101 camera system, and Barnes 12-1000 radiometer. The unit is simple to operate in the field offering the untrained user easy operation. Low power consumption makes operation with battery power possible.

Revised Design

Several more data loggers are to be built by LARS over the next year. There is to be a total of four more instruments built with six memory modules. The circuits for the revised units are the same for the most part. The only major revisions are in the computer interface. The interface will no longer be opto-isolated in the new data

logger. The opto-isolators in the proto-type caused more problems than solutions. Without the isolators, considerable savings were realized since a power supply and several fairly expensive isolators were no longer necessary. The time clock received only some cosmetic changes. Standard divide by six counters will be utilized as opposed to to forming divide by six counters from decade counters. The clock generator will also be changed to permit the oscillator to run off of the 5 volt supply. This will reduce wiring and power consumption of the clock. The multiplexer will be changed to a set of tri-state output buffers. One for each digital output word. This was done to permit easier layout. The largest change will be in the physical layout, both internally and externally. A standard zero case will be modified to be the chassis. The bottom piece will contain the data logger while the lid will contain the detachable memory module. The internal parts of the data logger will be drastically altered as well. Two 60 conductor ribbon cables with card edge connectors will form the bus for the revised unit. This will offer considerably easier wiring of the new unit. The number of PC boards in the new unit will also be reduced in an effort to reduce wiring and ease construction. The result of the redesign will be a considerably smaller package. The new unit will be 13.25 x 9.2 x 11.75 inches, with the memory module.

LIST OF REFERENCES

LIST OF REFERENCES

F. E. Nicodemus, J. C. Richmond, and J. J. Hsia, "Geometrical Considerations and Nomenclature For Reflectance", NBS MONOGRAPH 160, National Bureau of Standards, U. S. Department Of Commerce, October 1977

APPENDICES

APPENDIX A

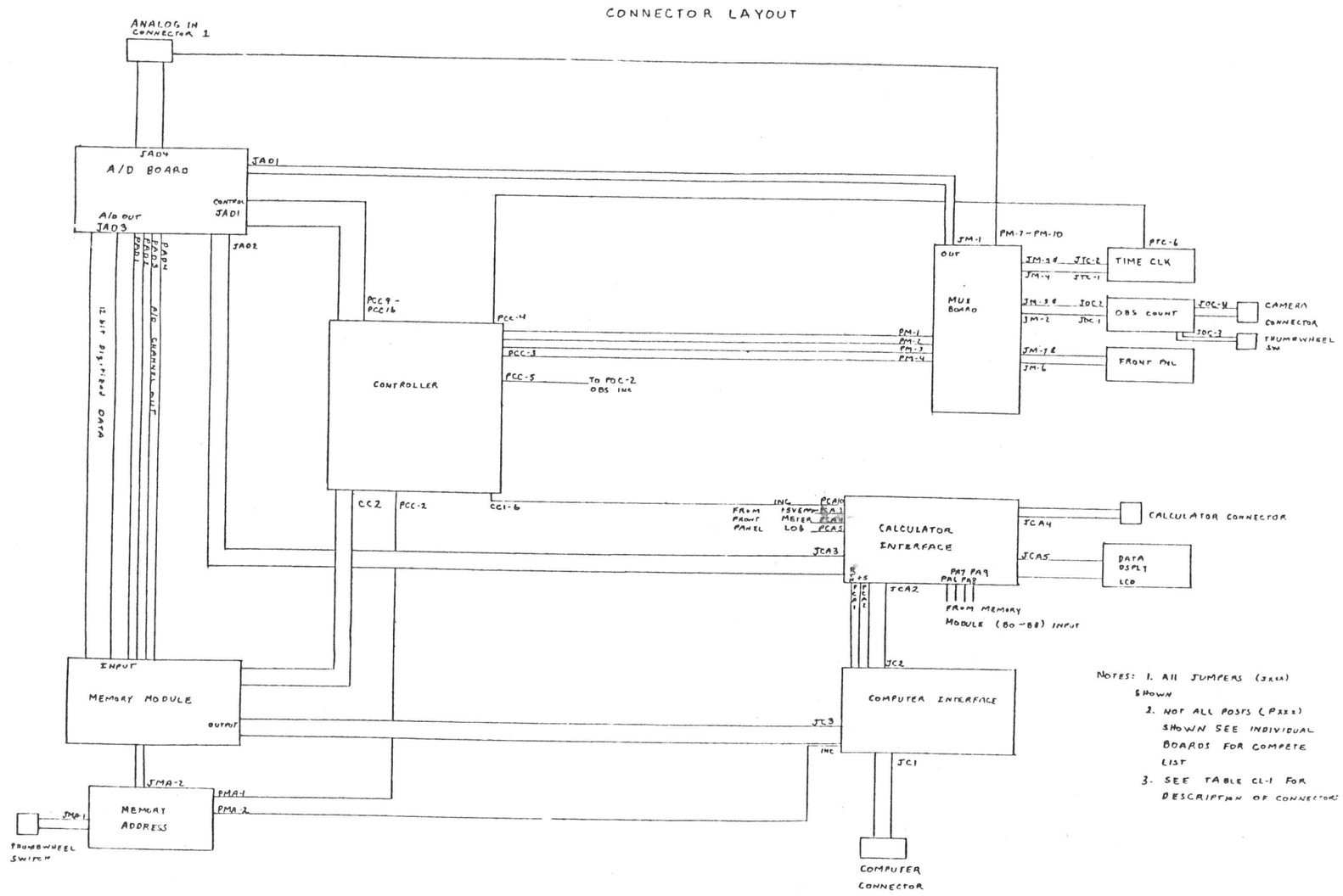


Figure A-1. Interconnect Layout

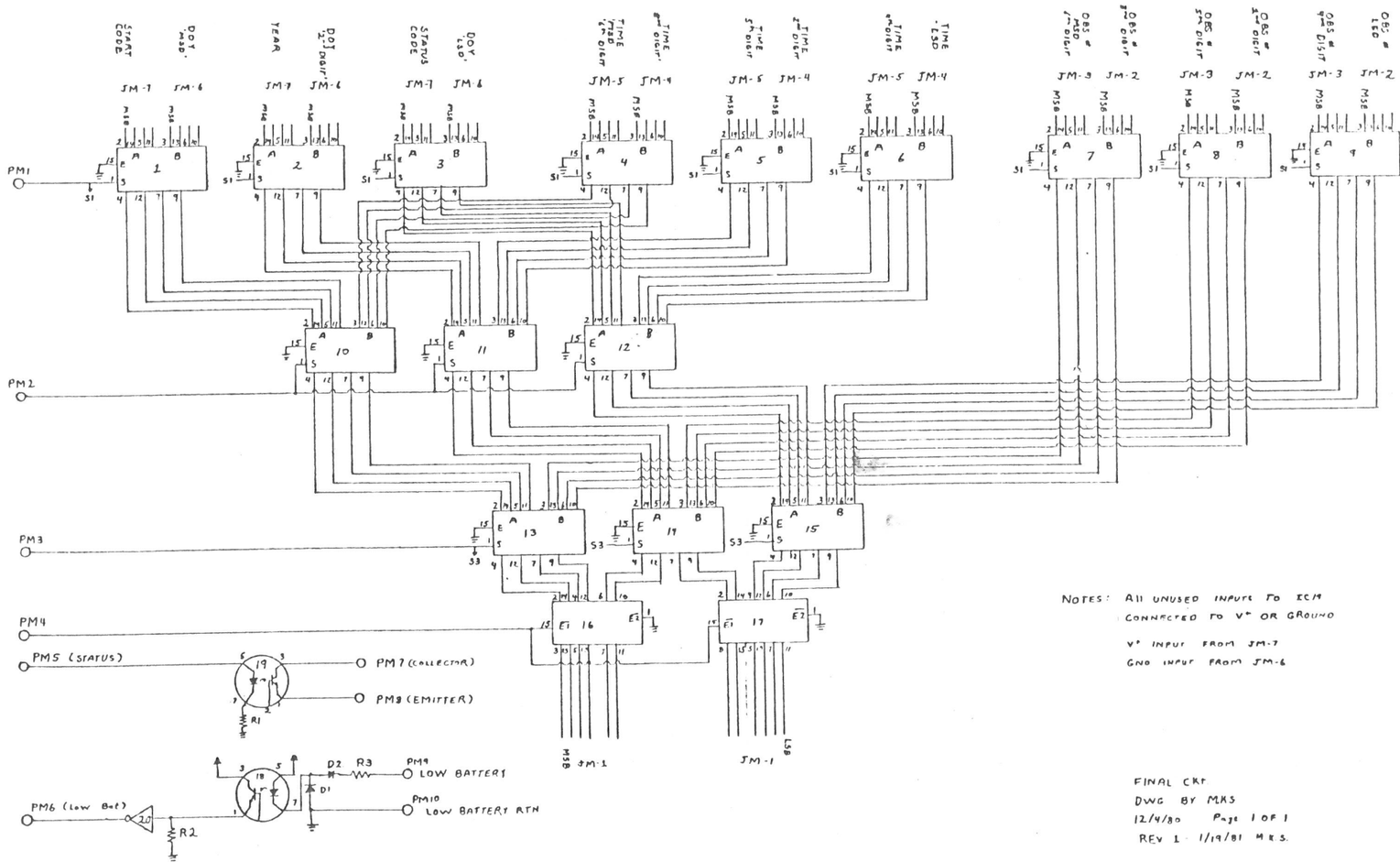


Figure A-2. Radiometer Interface/Multiplexer

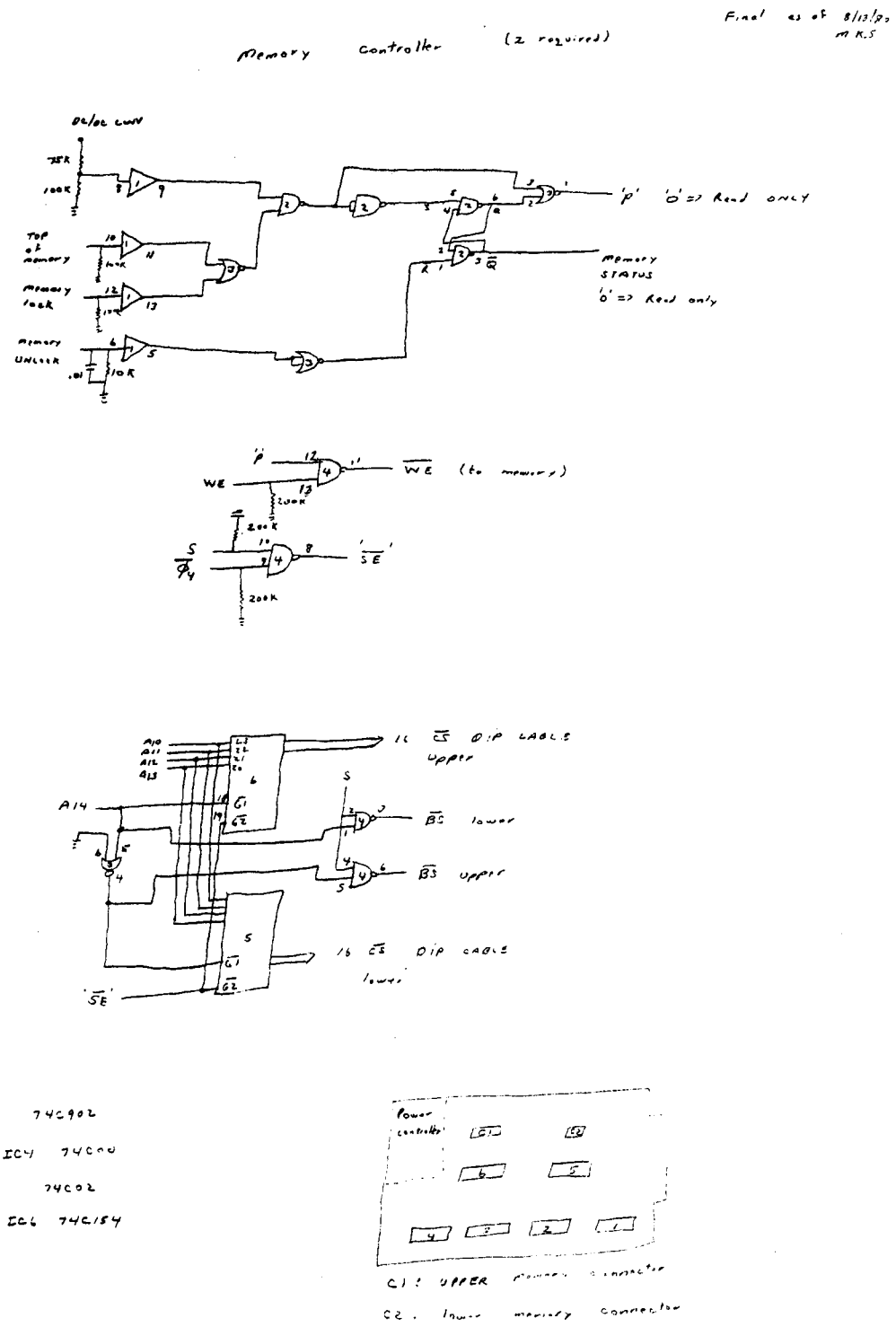
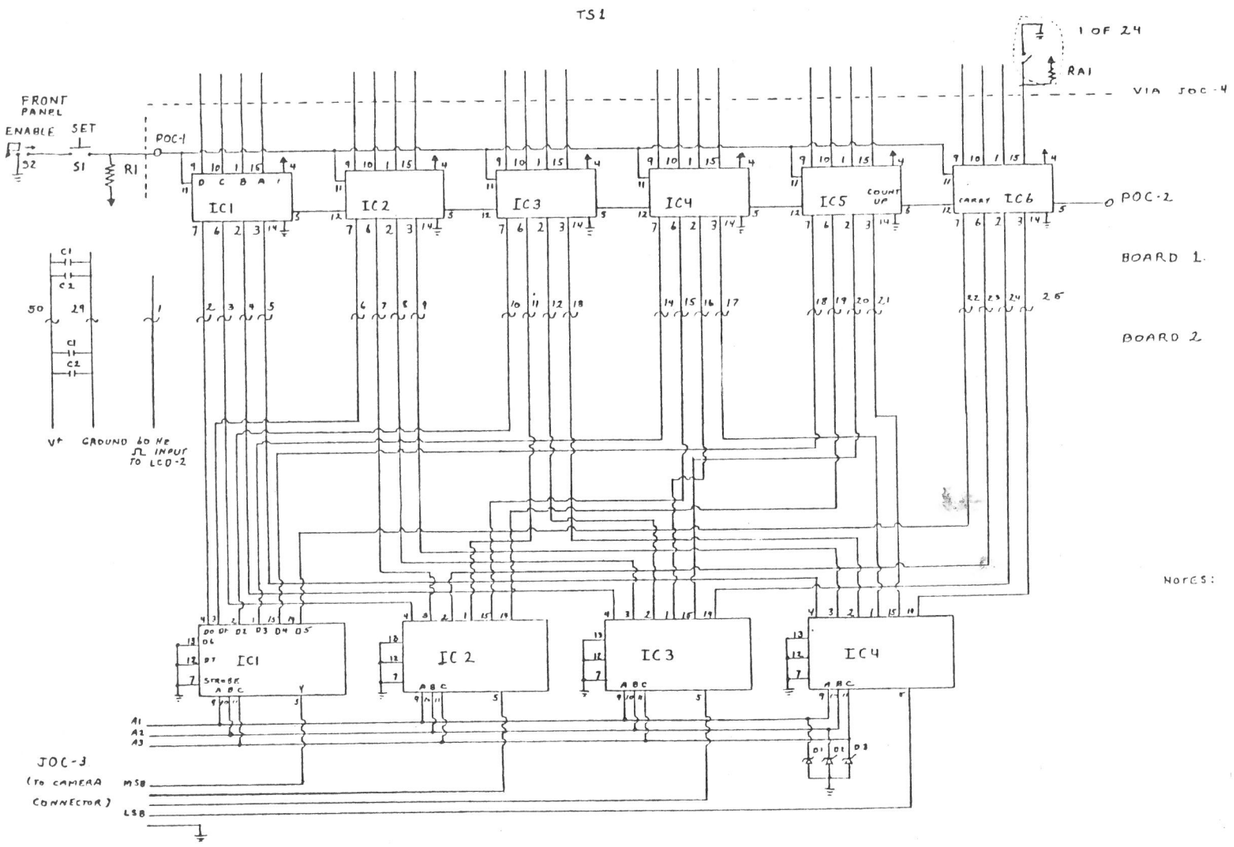


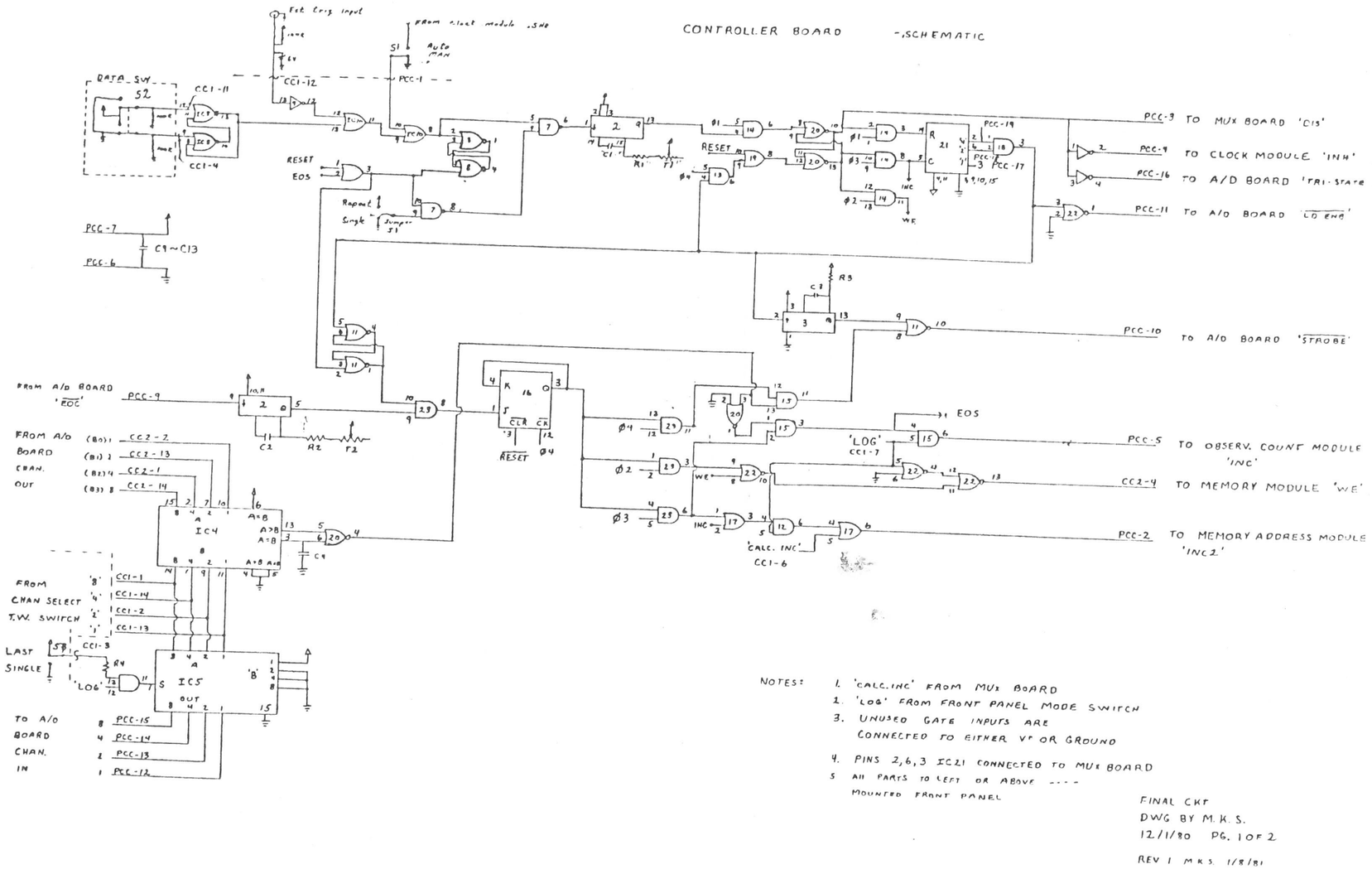
Figure A-3. Memory Controller



NOTES:
1. ~ INDICATES INTERBOARD CONNECTOR. INTERBOARD CONNECTOR CONNECTS OC-2 TO OC-1 TO LCD-2
2. TS1, S1, S2, RA1-RA6 MOUNTED FRONT PANEL

FINAL CKT
DWG BY M.K.S
12-15-80 PG 1 OF 1

Figure A-4. Observation Counter



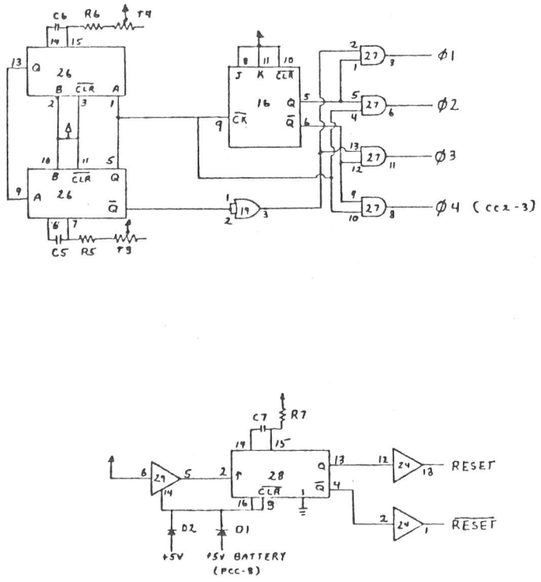
NOTES:

1. 'CALC.INC' FROM MUX BOARD
2. 'LOG' FROM FRONT PANEL MODE SWITCH
3. UNUSED GATE INPUTS ARE CONNECTED TO EITHER V+ OR GROUND
4. PINS 2,6,3 IC21 CONNECTED TO MUX BOARD
5. ALL PARTS TO LEFT OR ABOVE ---- MOUNTED FRONT PANEL

FINAL CKT
DWG BY M.K.S.
12/1/80 PG. 1 OF 2
REV 1 M.K.S. 1/8/81

Figure A-5. Controller

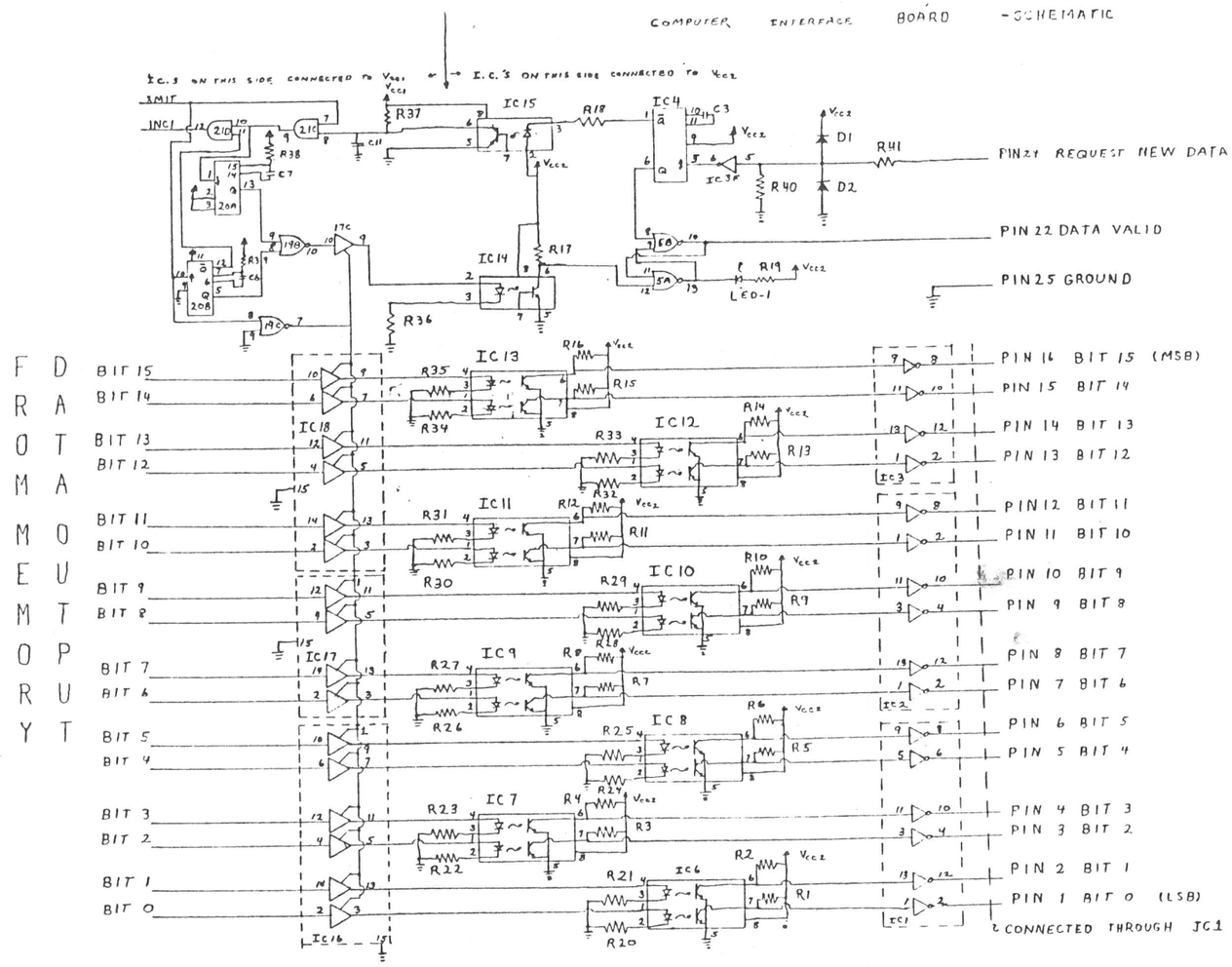
CONTROLLER BOARD -SCHEMATIC



NOTES: 5V BATTERY SAME AS CLOCK BATTERY

FINAL CKT.
DWG. BY M. K. S.
12/1/80 PG 2 OF 2.

Figure A-6. Clock Generator



NOTE: R41 MOUNTED ON DELTA CONN.

NOTE: TTL GROUND CONNECTED TO COMPUTER CHASSIS

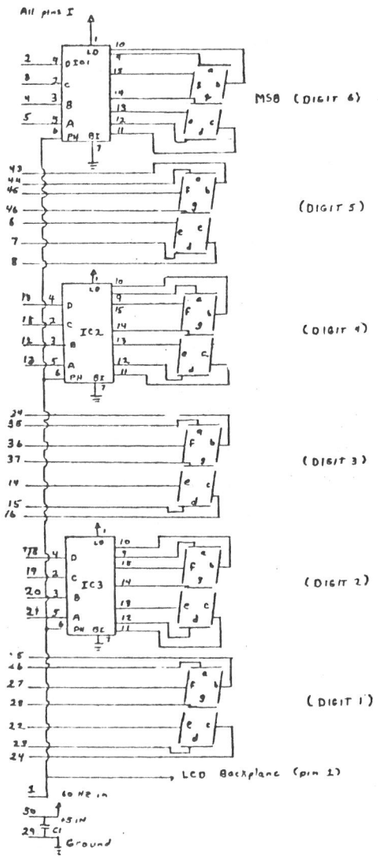
FINAL CKT
DWG BY M.K.S.
10/2/80

PG 1 of 2

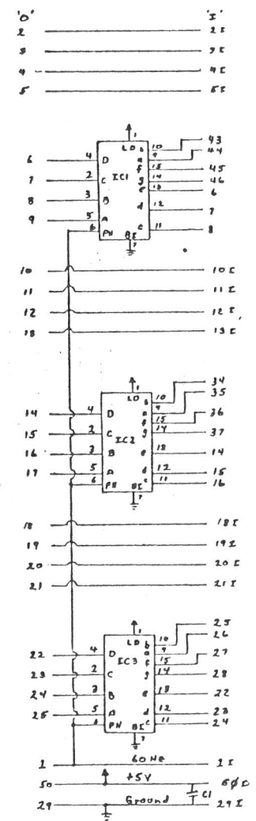
Figure A-7. Computer Interface

LCD DISPLAY DRIVER BOARD -SCHEMATIC
(3 SETS REQUIRED)

LCD BOARD 1



LCD BOARD 2



NOTES: 1: SEE LCD PINOUT FOR LCD PIN NUMBERS

2: ON DATA DISPLAY ONLY ADD .001 mF between LCD pin 33 and Ground (adds colon)

FINAL CKT
DWG. BY M.K.S.
11/18/80 PG 1 OF 1

Figure A-8. LCD Driver

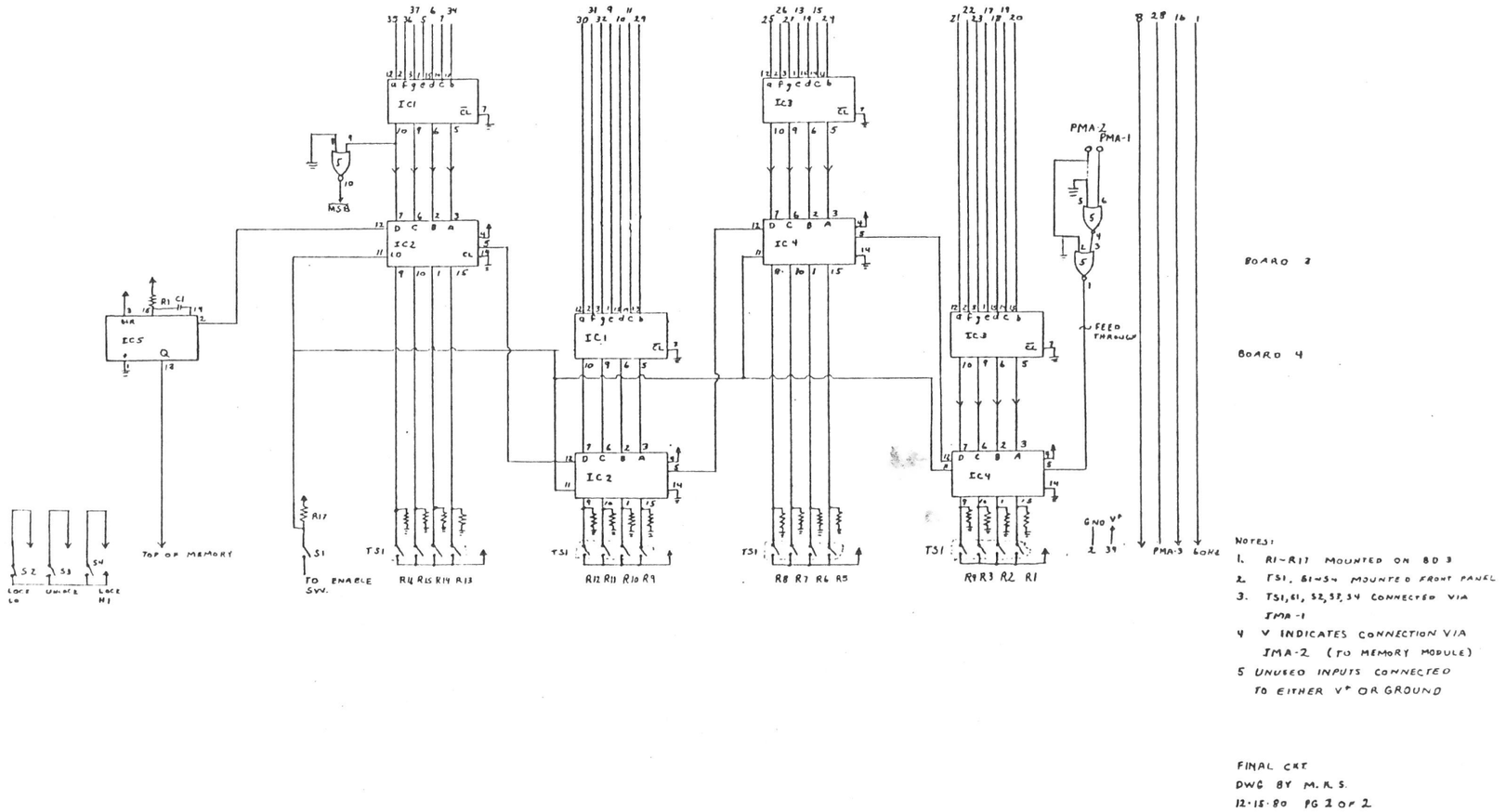


Figure A-9. Memory Pointer

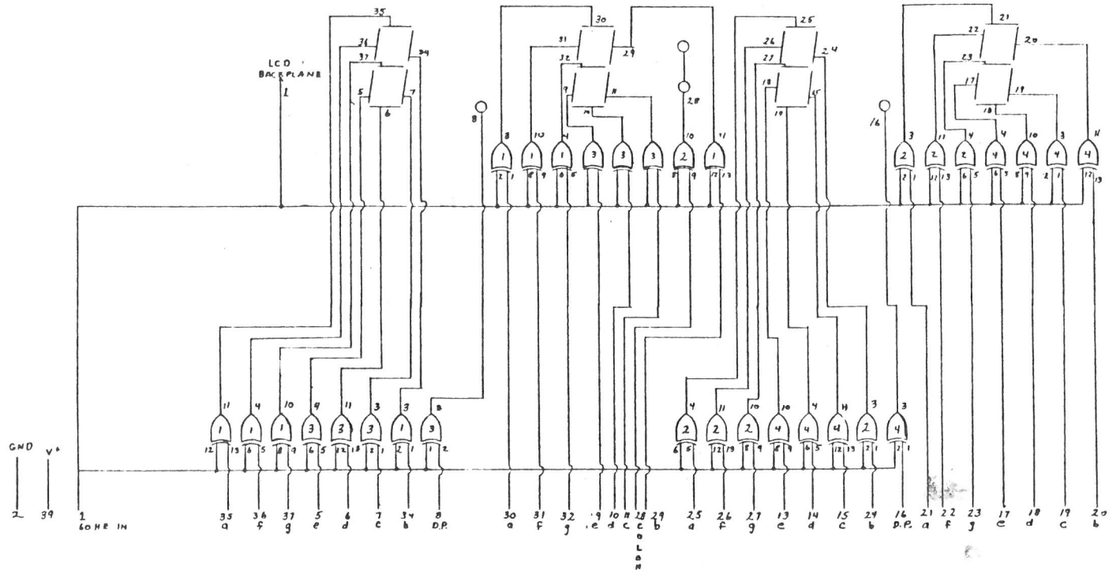


Figure A-10. Memory Pointer Display Driver

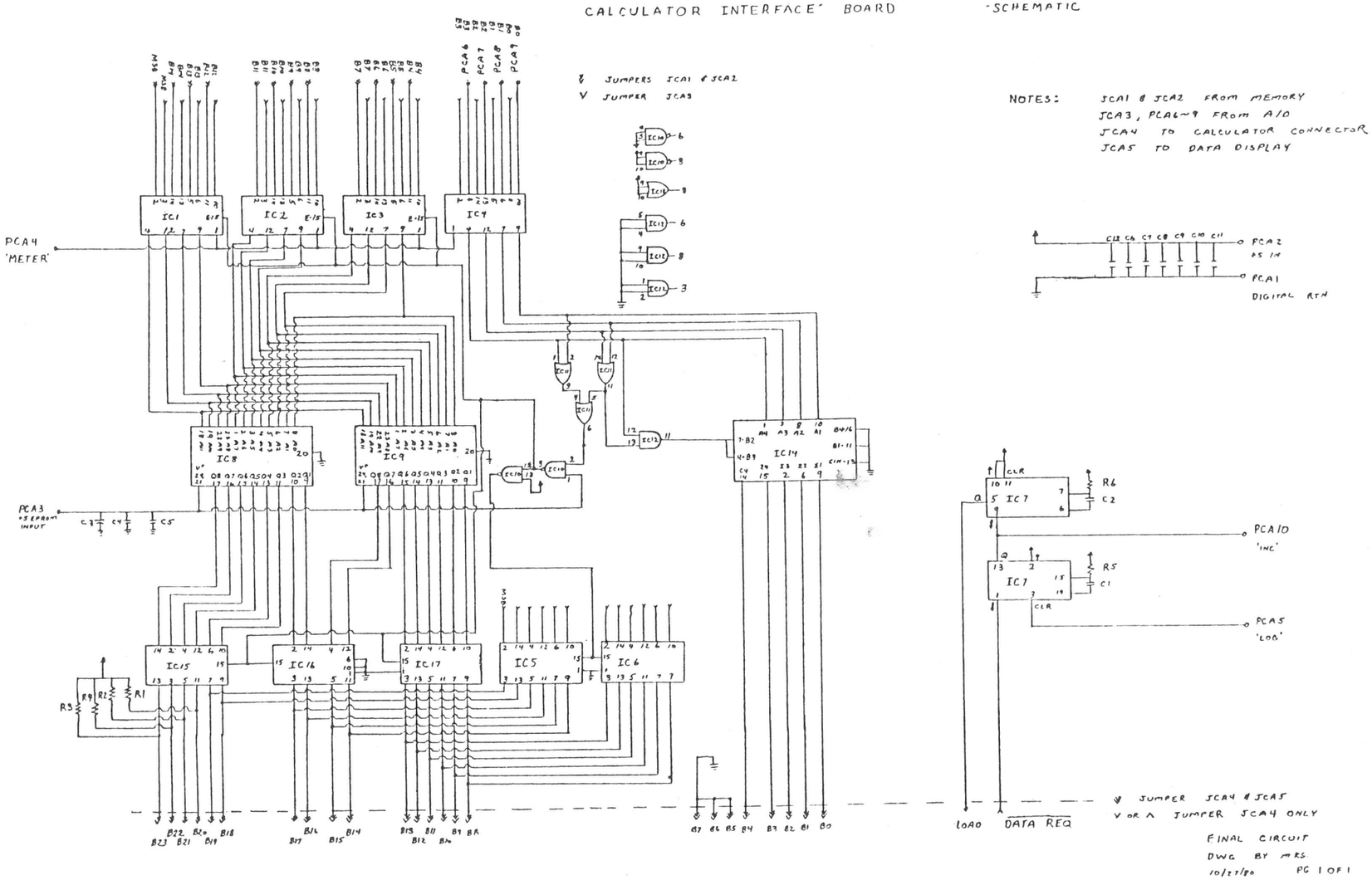
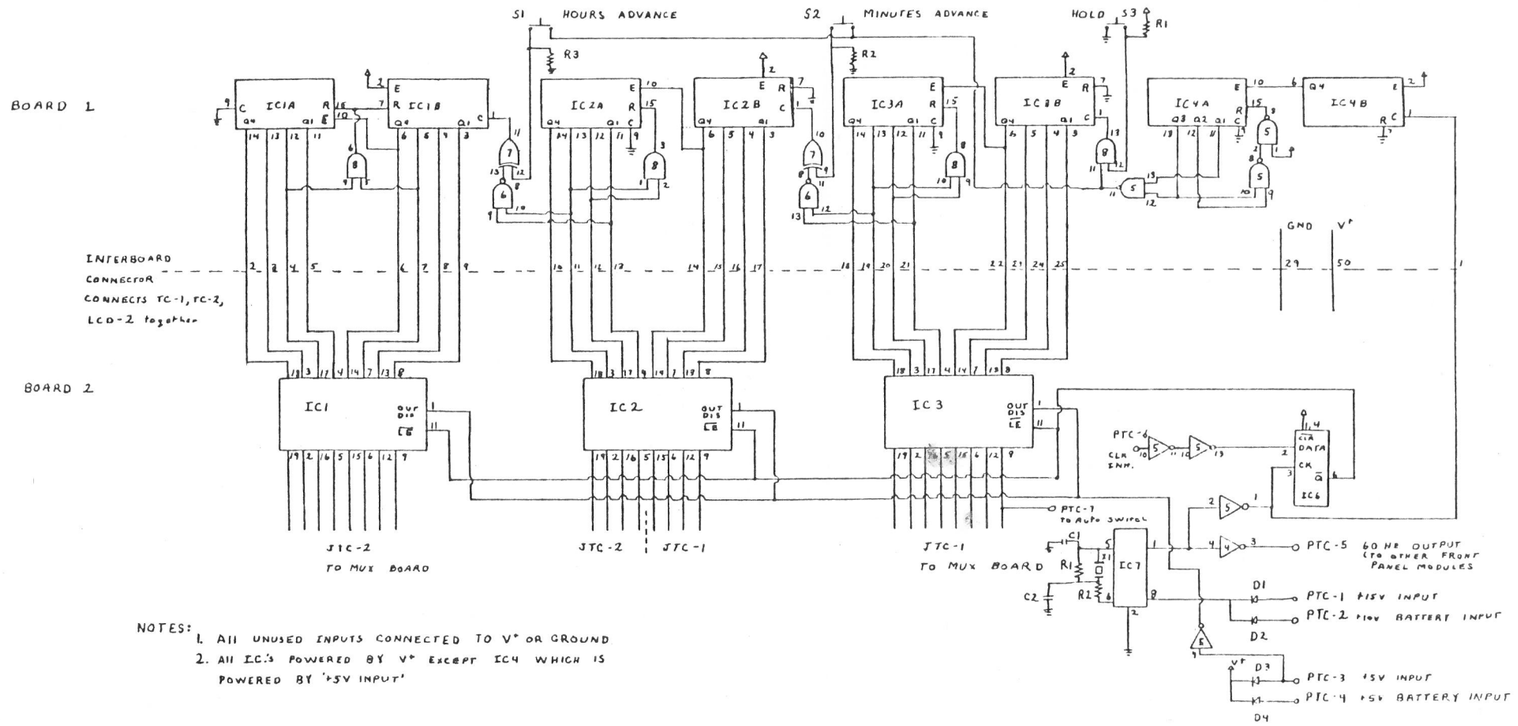


Figure A-11. Display/Calculator Interface

TIME CLOCK BOARDS 1&2 - SCHEMATIC

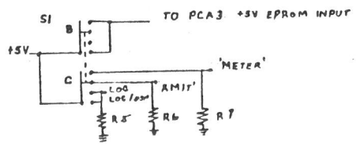


NOTES:
1. All unused inputs connected to V+ or ground
2. All IC's powered by V+ except IC4 which is powered by '+5V input'

FINAL CKT
DWG BY M.K.S.
12/11/80 PG. 1 OF 1

Figure A-12. Time Clock

FRONT PANEL (PARTS NOT SHOWN ELSEWHERE ONLY) -SCHEMATIC



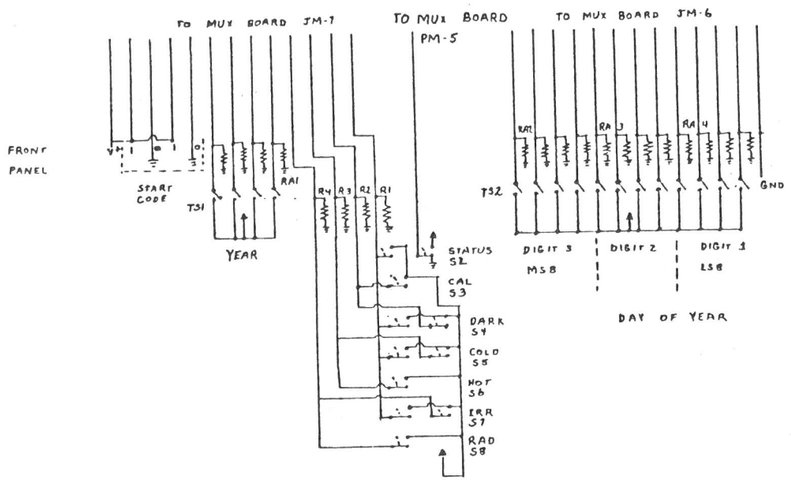


Figure A-13. Front Panel Circuitry

NOTES: 1. S1 DESCRIBED IN COMPUTER INTERFACE C.F. S1A
2. S2-S8 SHOWN IN NORMAL POSITION

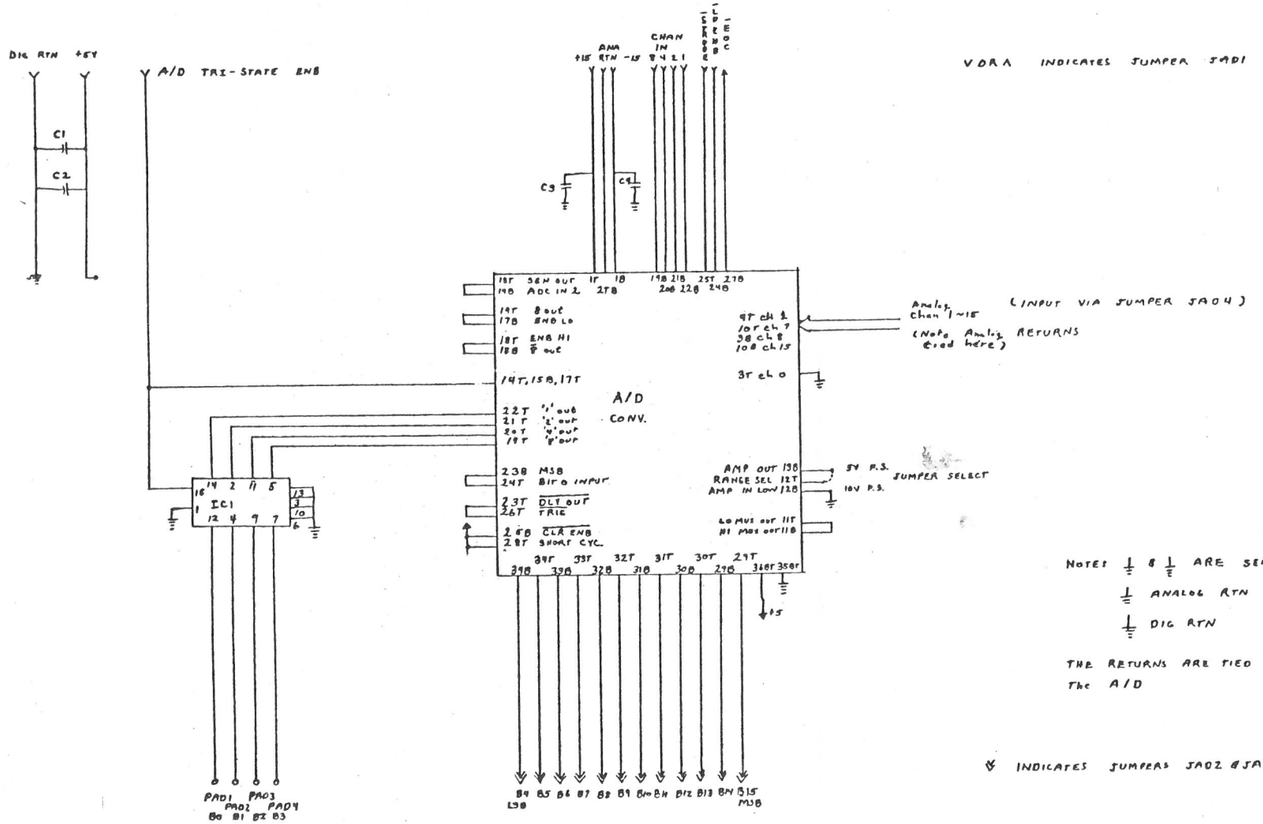
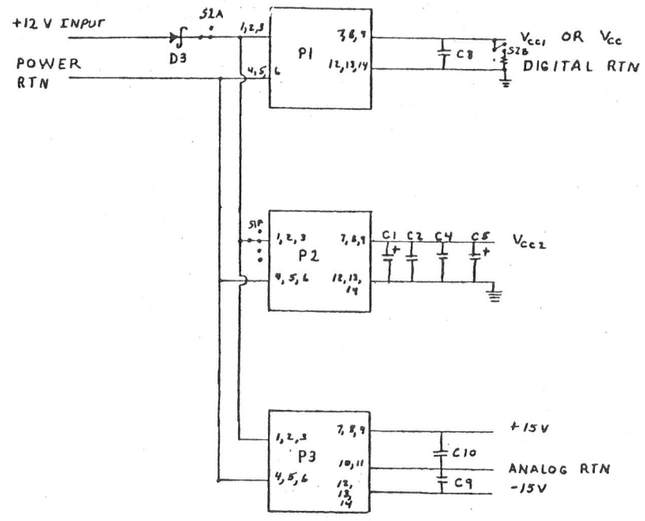


Figure A-14. A/D Converter

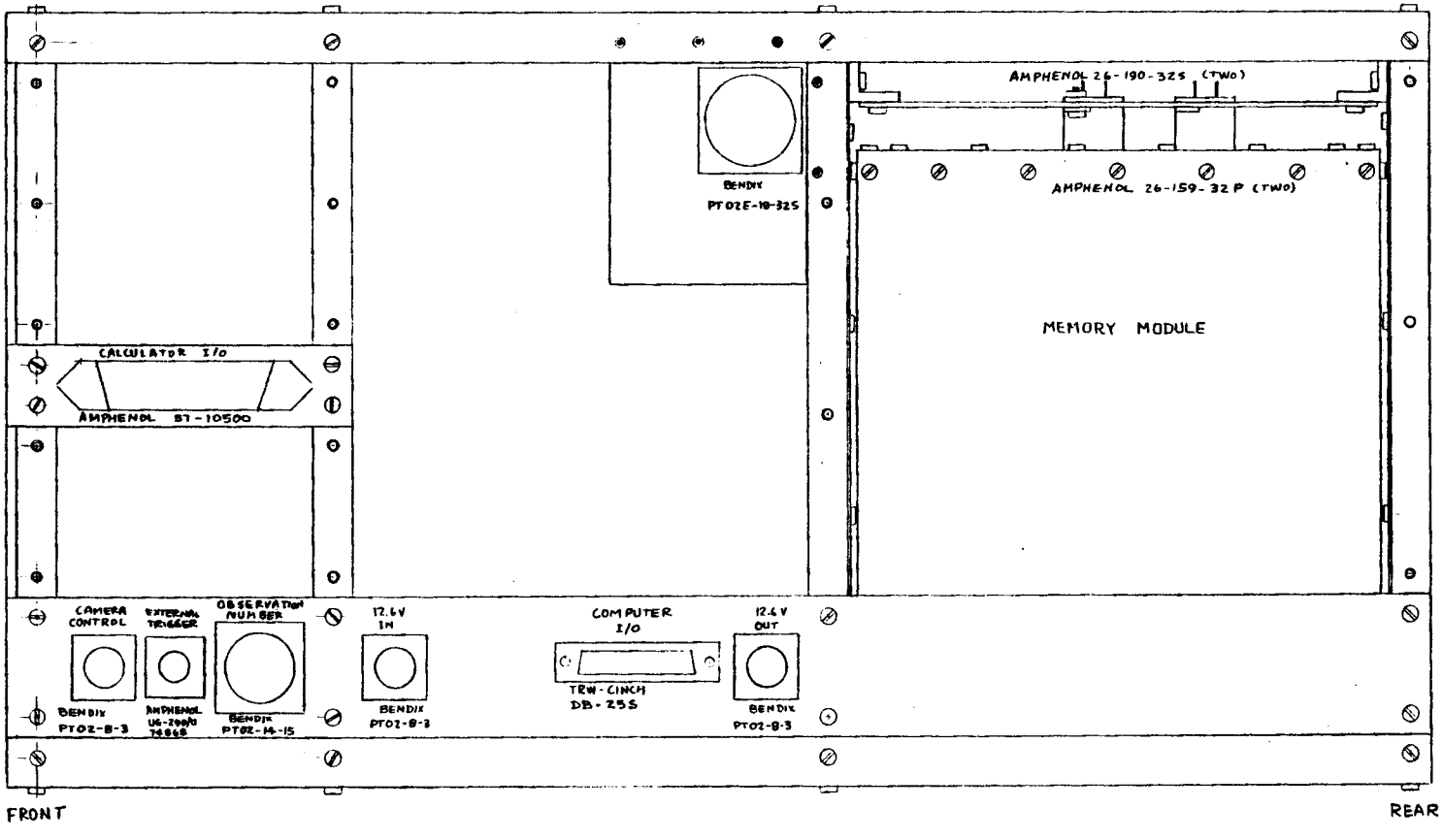
COMPUTER INTERFACE BOARD - SCHEMATIC



NOTES: S1, S2 MOUNTED FRONT PANEL
S1 SHOWN IN XMIT MODE
S2 SHOWN IN 'ON' MODE

FINAL CKT
DWG BY M.K.S.
10/2/80
PG 2 OF 2

Figure A-15. Power Supplies



CH-1A. CONNECTOR AND SUB-ASSEMBLY LAYOUT
BOX LEFT-SIDE VIEW

Figure A-16. Chassis Side View

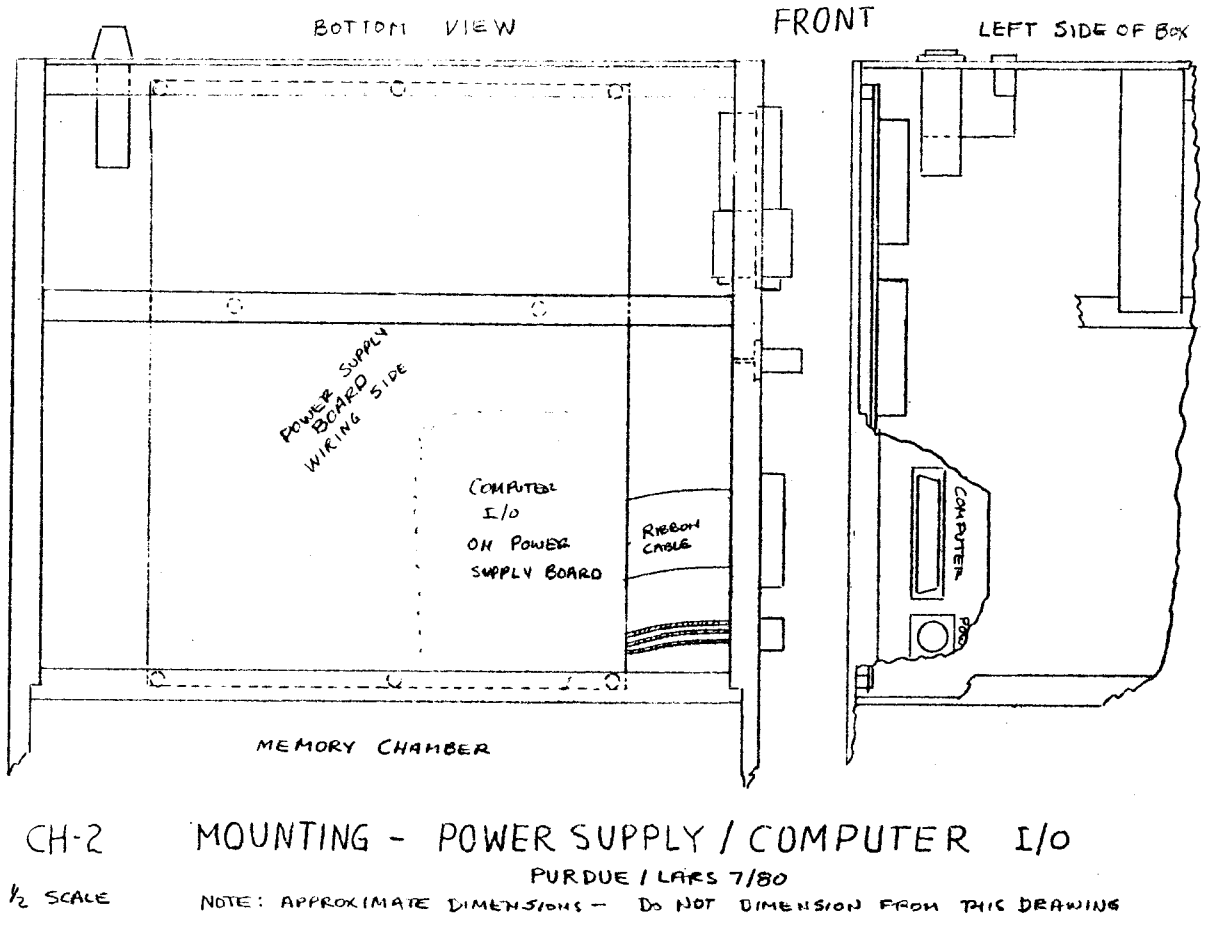


Figure A-17. Chassis Bottom View

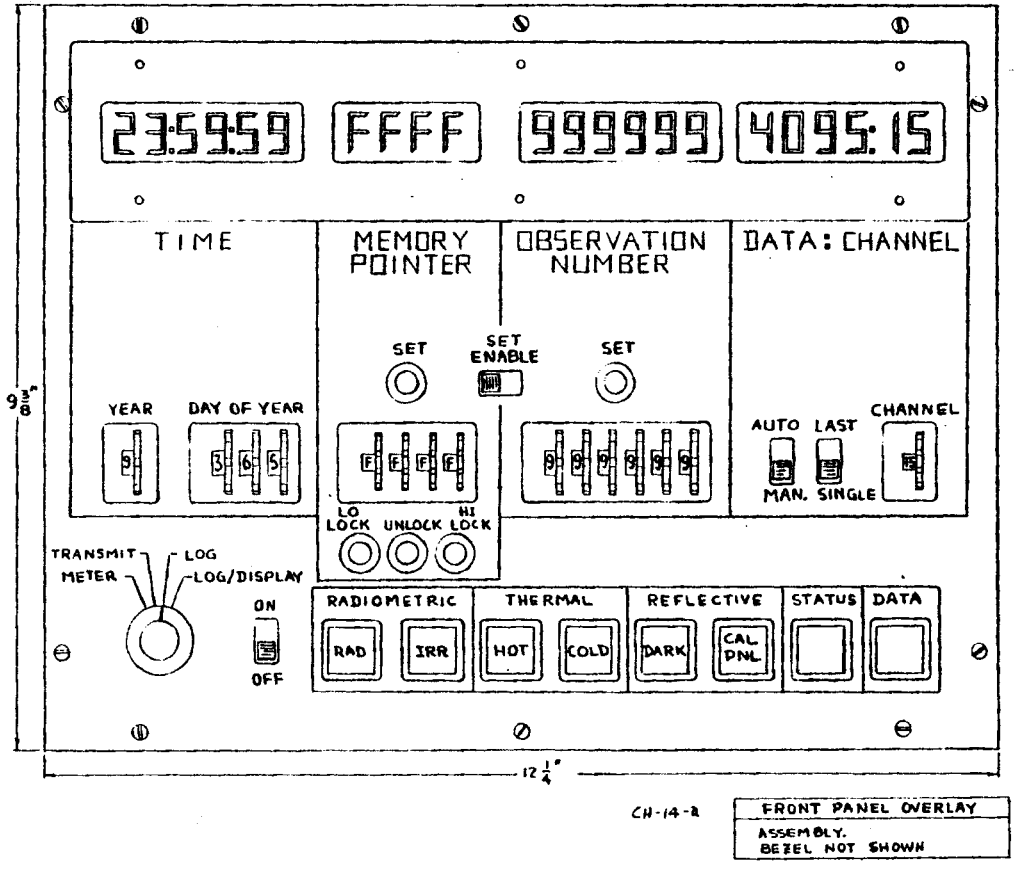


Figure A-18. Chassis Front View

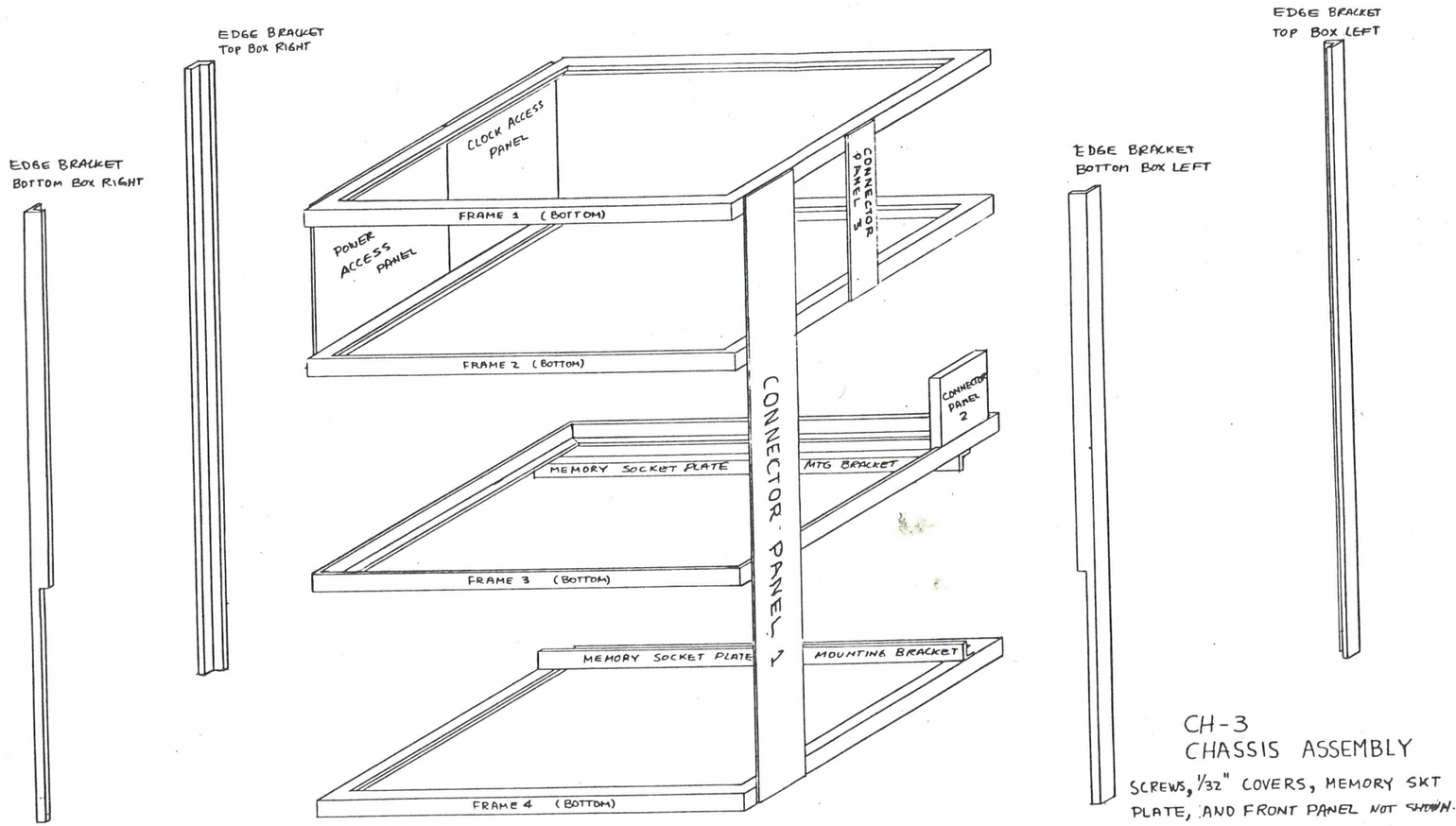
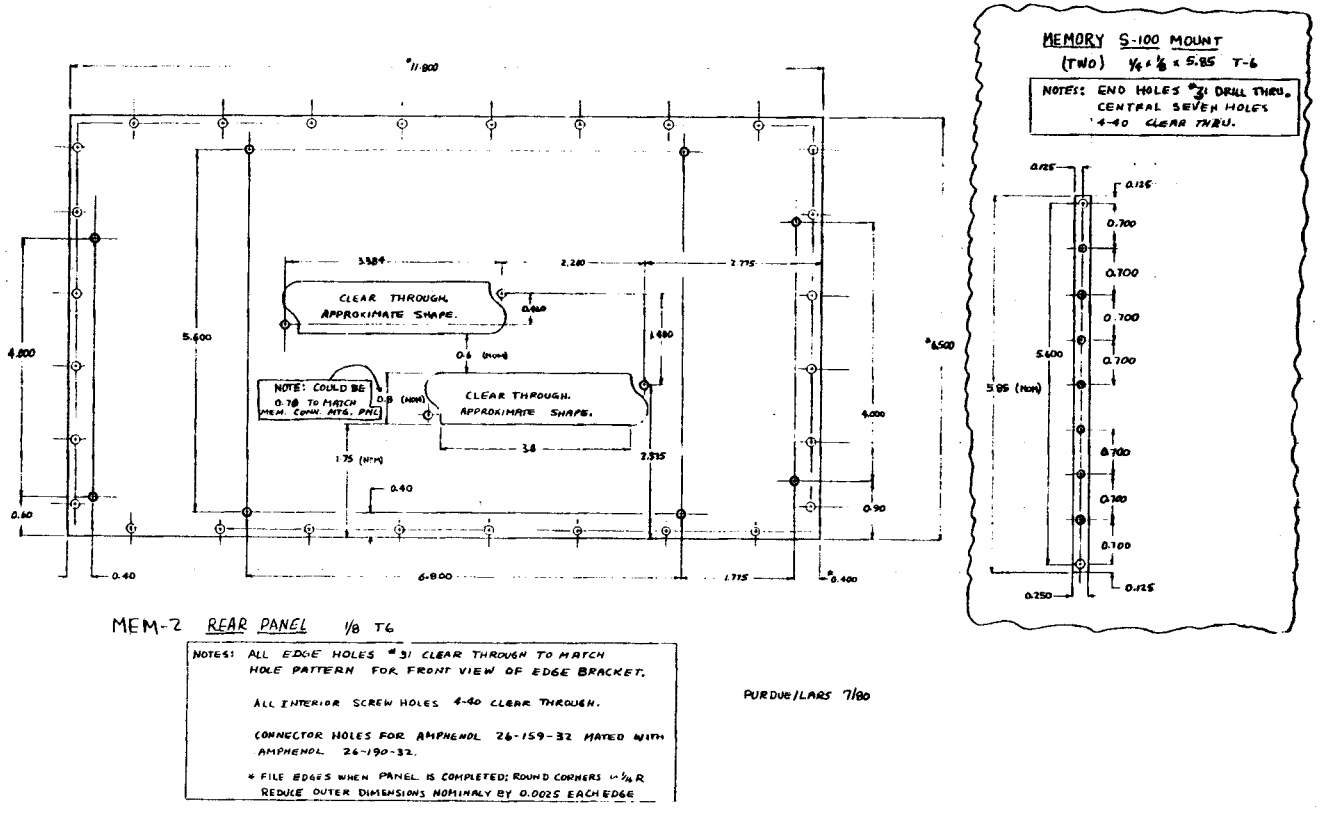


Figure A-19. Chassis Assembly



MEM-2 REAR PANEL 1/8 T6

NOTES: ALL EDGE HOLES #31 CLEAR THROUGH TO MATCH HOLE PATTERN FOR FRONT VIEW OF EDGE BRACKET.

ALL INTERIOR SCREW HOLES 4-40 CLEAR THROUGH.

CONNECTOR HOLES FOR AMPHENOL 26-159-32 MATED WITH AMPHENOL 26-190-32.

* FILE EDGES WHEN PANEL IS COMPLETED; ROUND CORNERS w/ ⅛ R
REDUCE OUTER DIMENSIONS NOMINALLY BY 0.002S EACH EDGE

PURDUE/LARS 7/80

Figure A-20. Memory Connector Panel

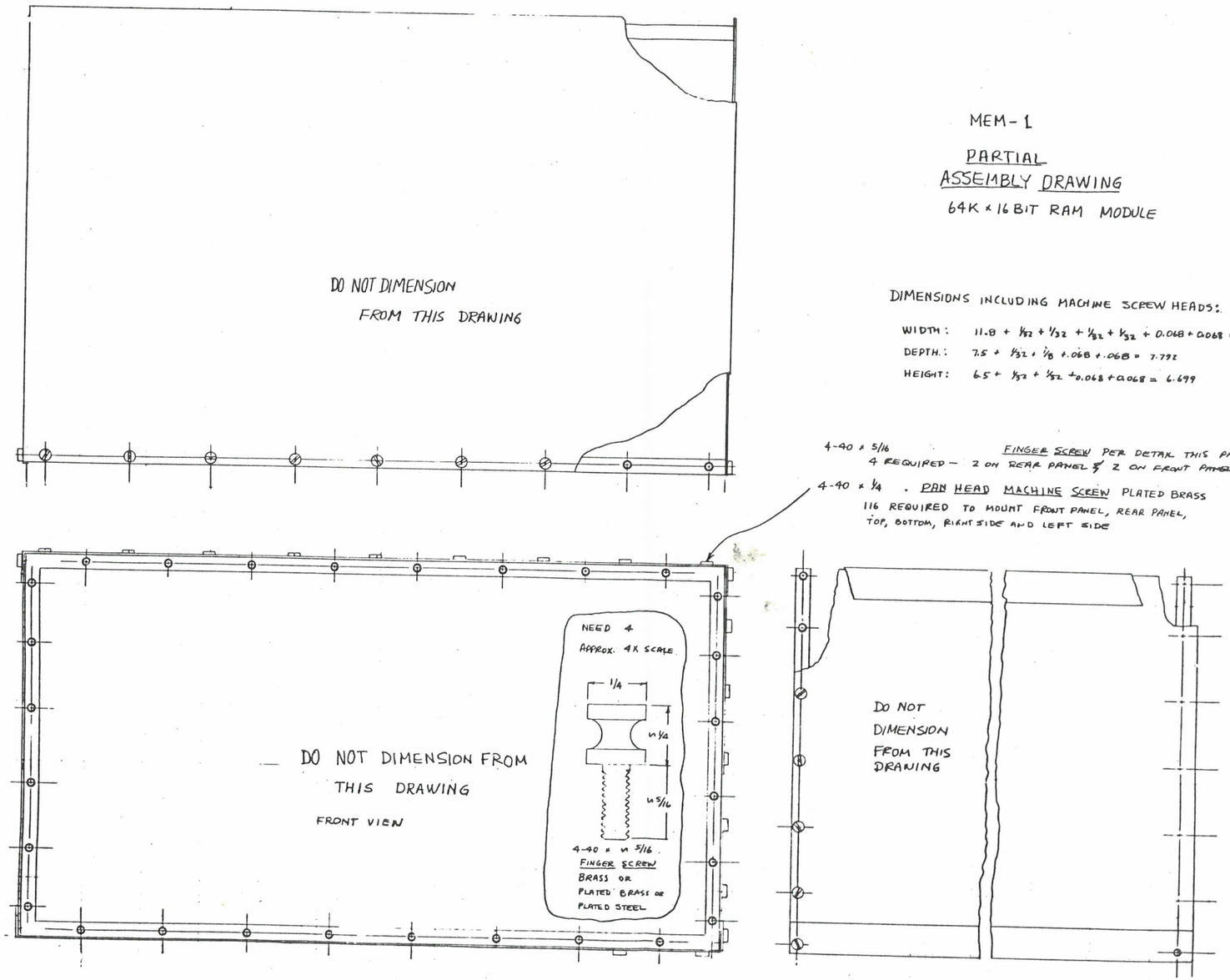


Figure A-21. Memory Assembly

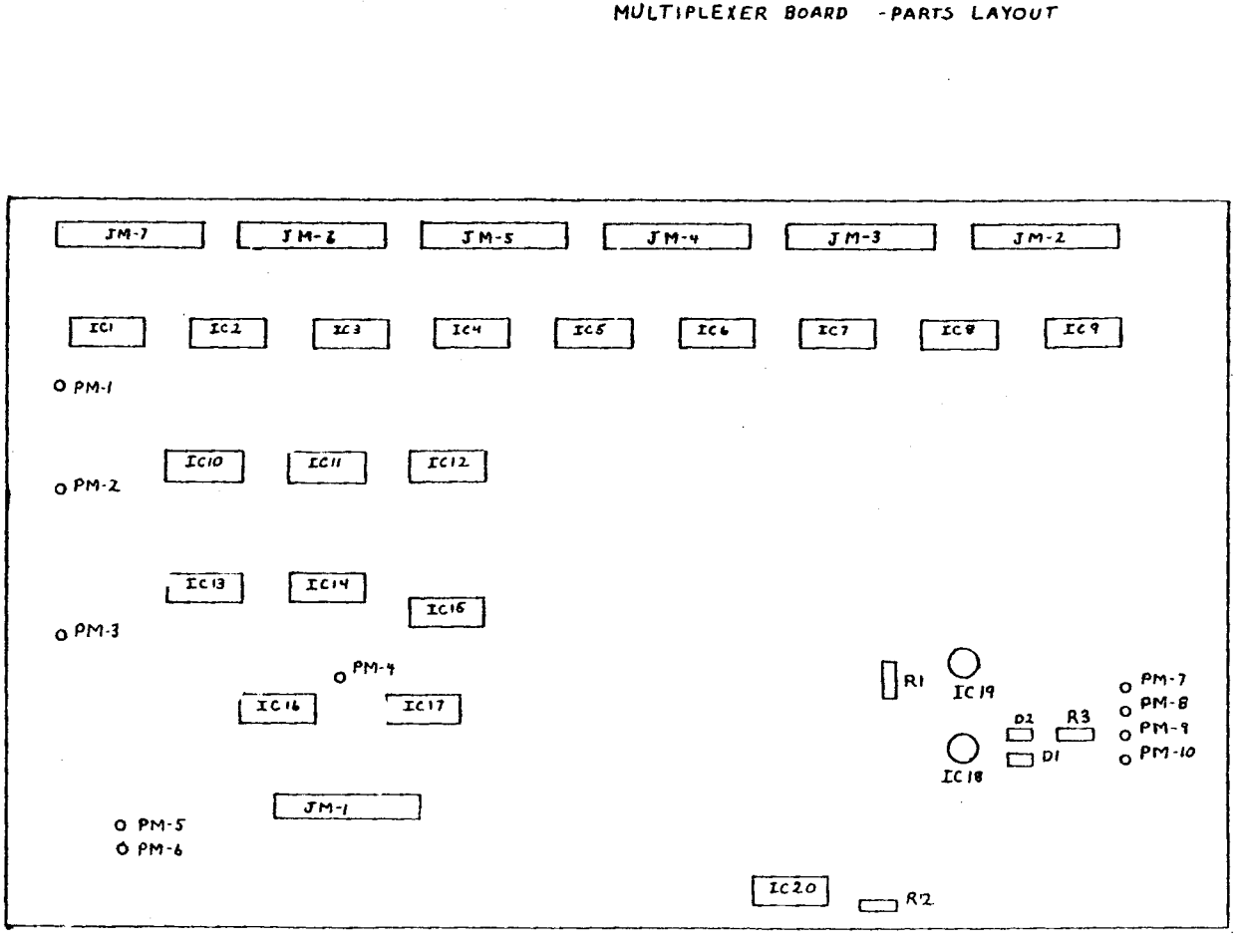


Figure A-22. Radiometer Interface/Multiplexer Layout

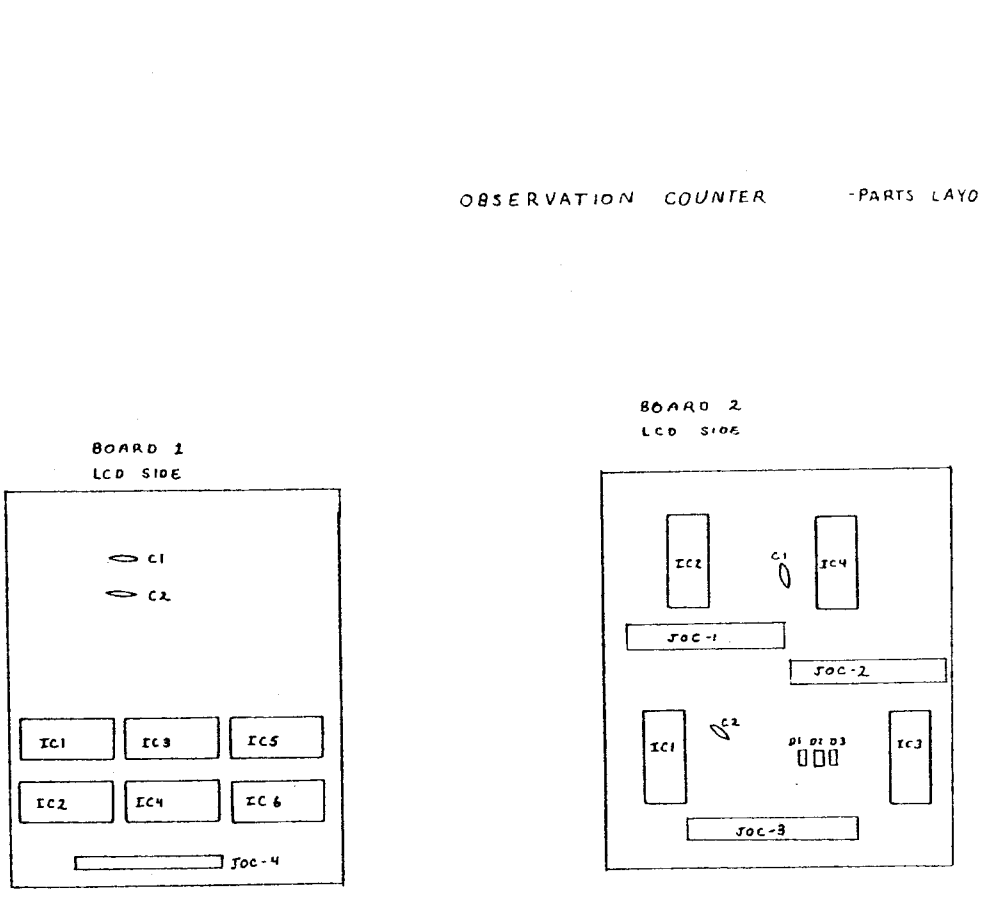


Figure A-23. Observation Counter Layout

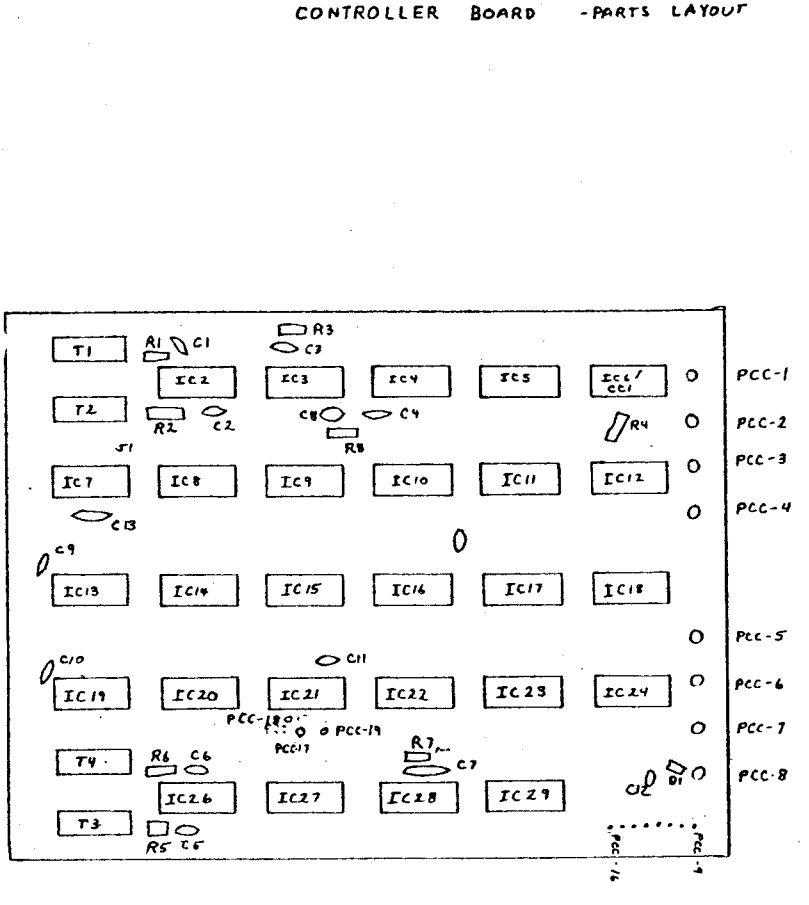
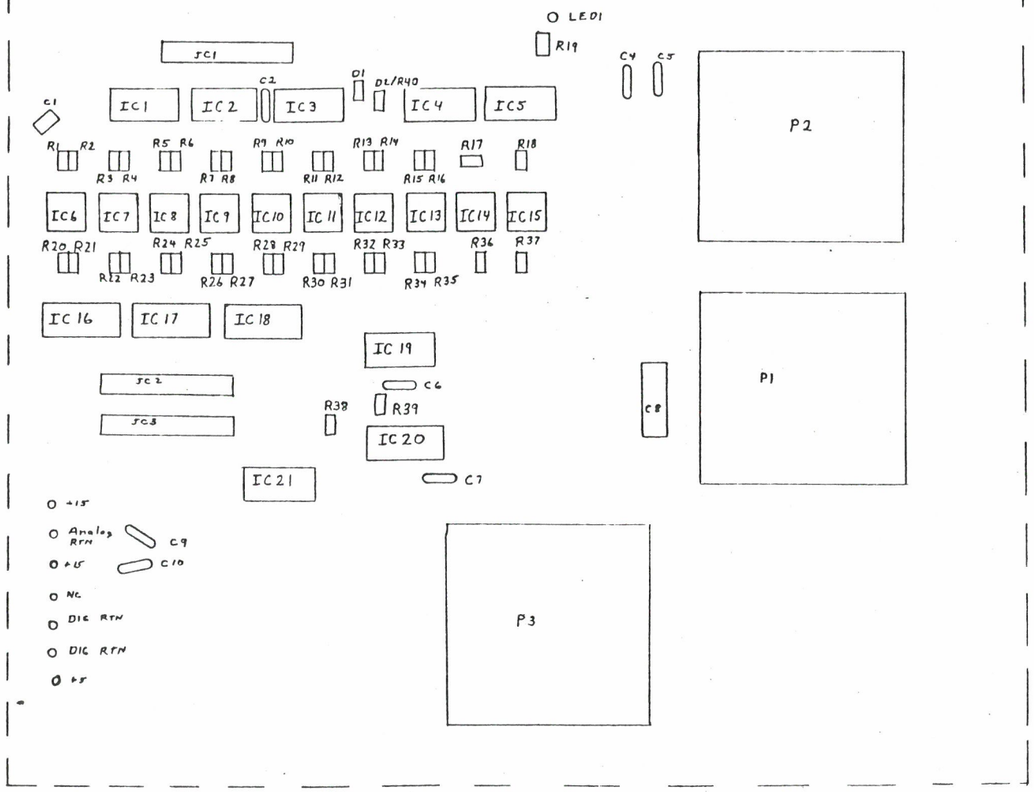


Figure A-24. Controller Layout

COMPUTER INTERFACE BOARD -PARTS LAYOUT



FINAL CKT
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10/5/80
PG 1 OF 1

Figure A-25. Computer Interface Layout

LCD DISPLAY DRIVER BOARD -PARTS LAYOUT
(2 SETS REQUIRED)

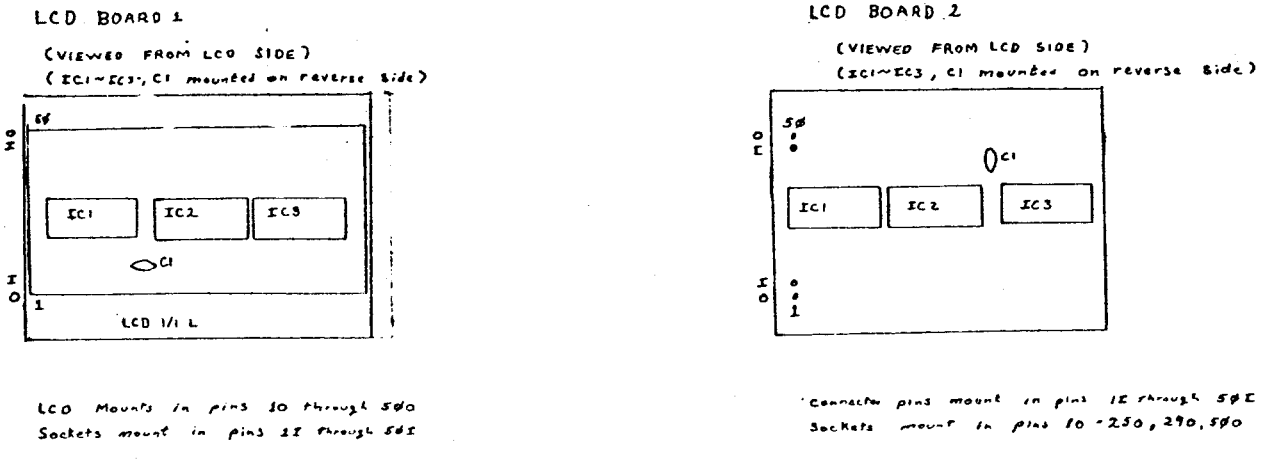

Figure A-26. LCD Driver Layout

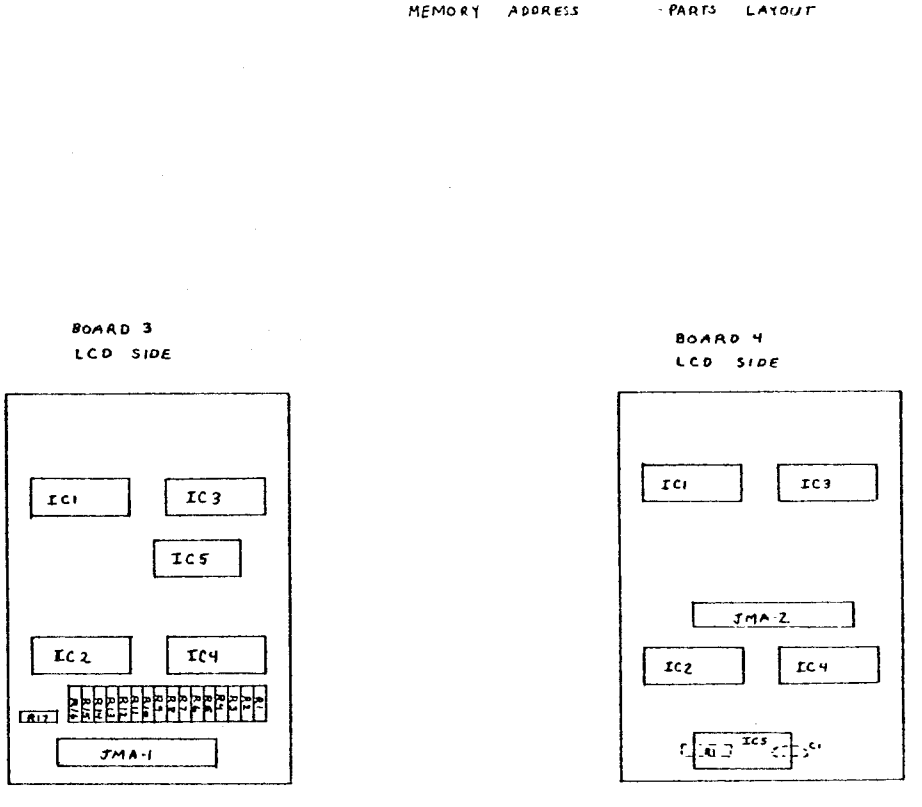

Figure A-27. Memory Pointer Layout

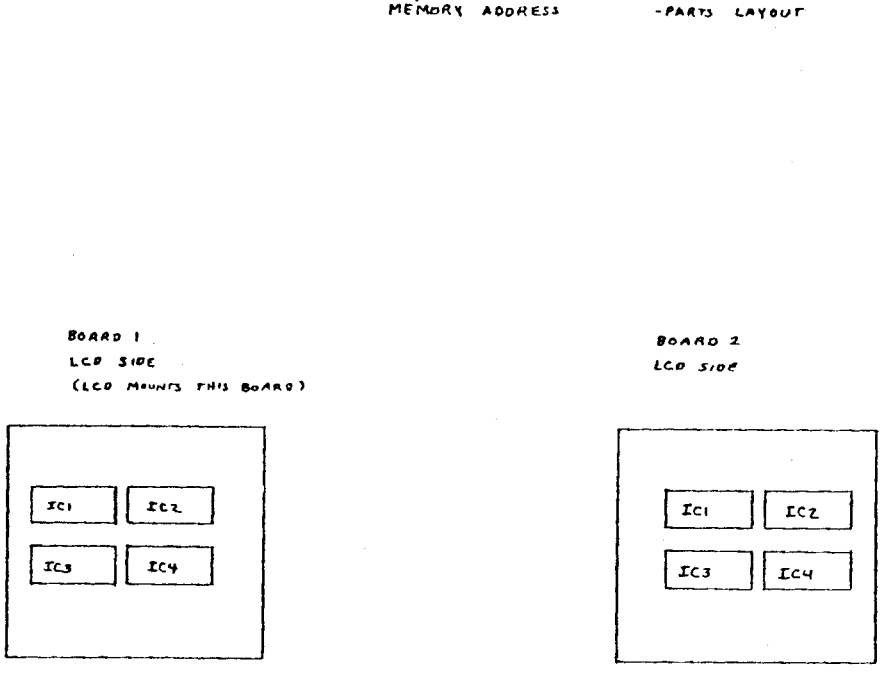

Figure A-28. Memory Pointer Display Driver Layout

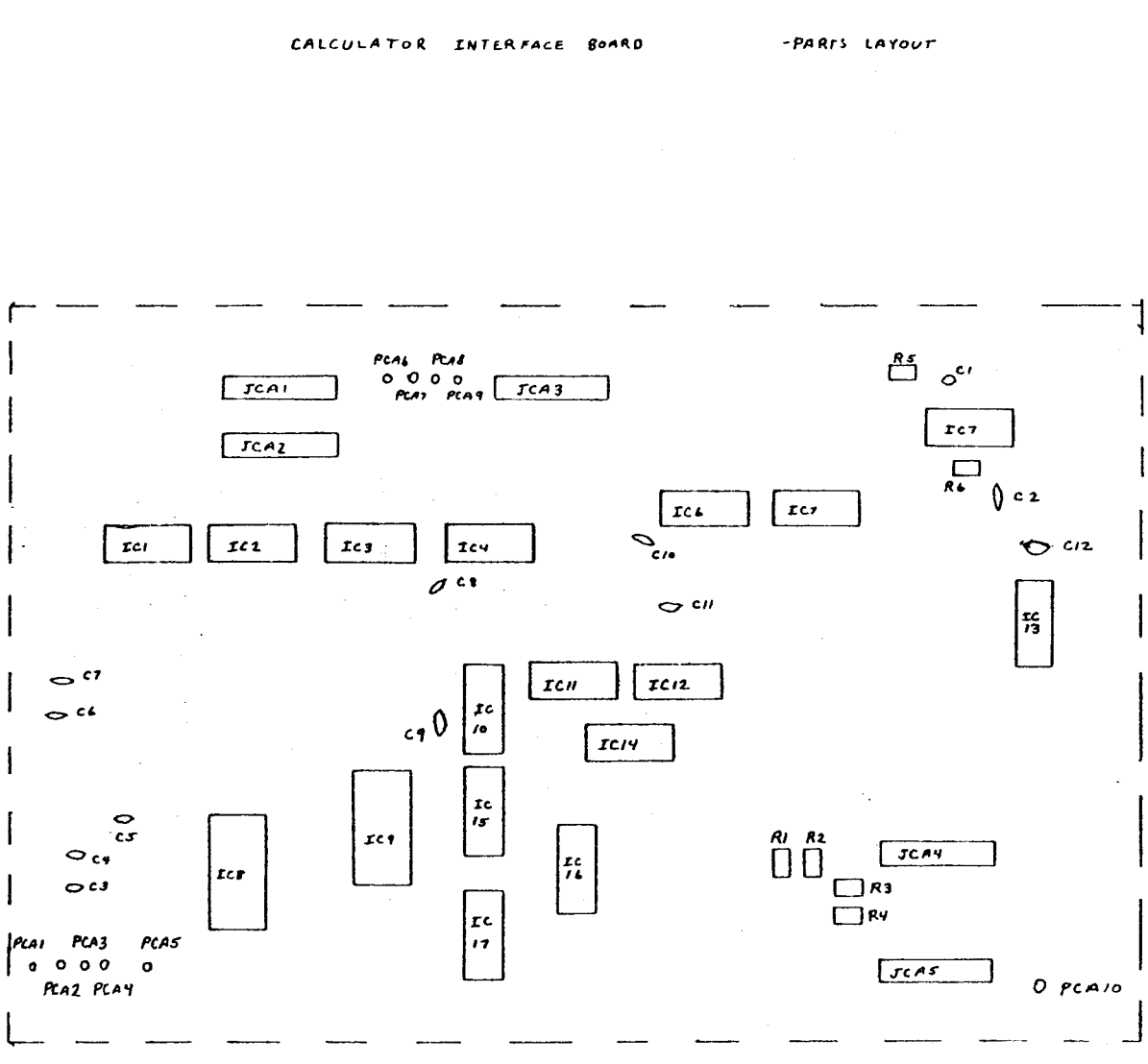

Figure A-29. Display/Calculator Interface Layout

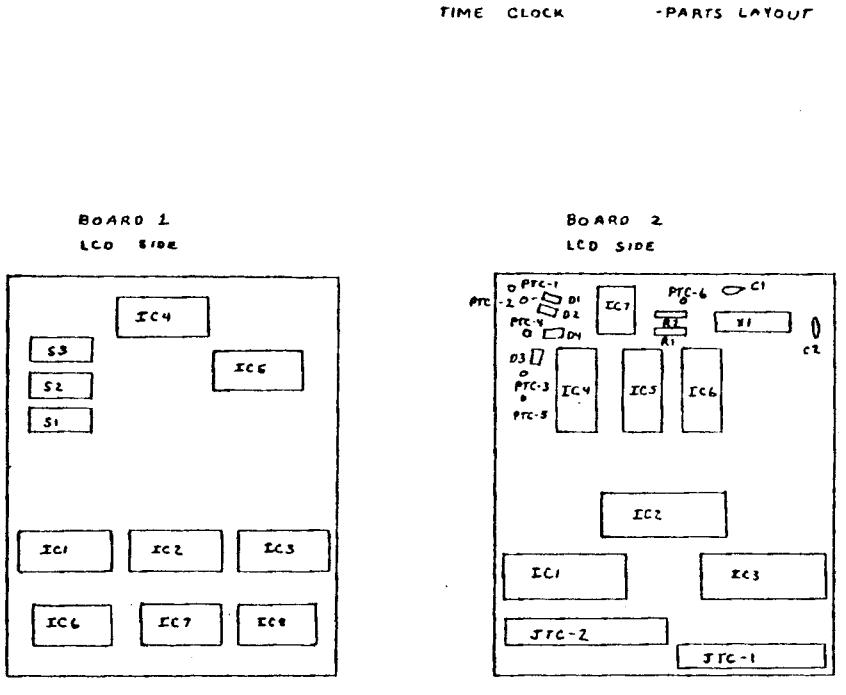

Figure A-30. Time Clock Layout

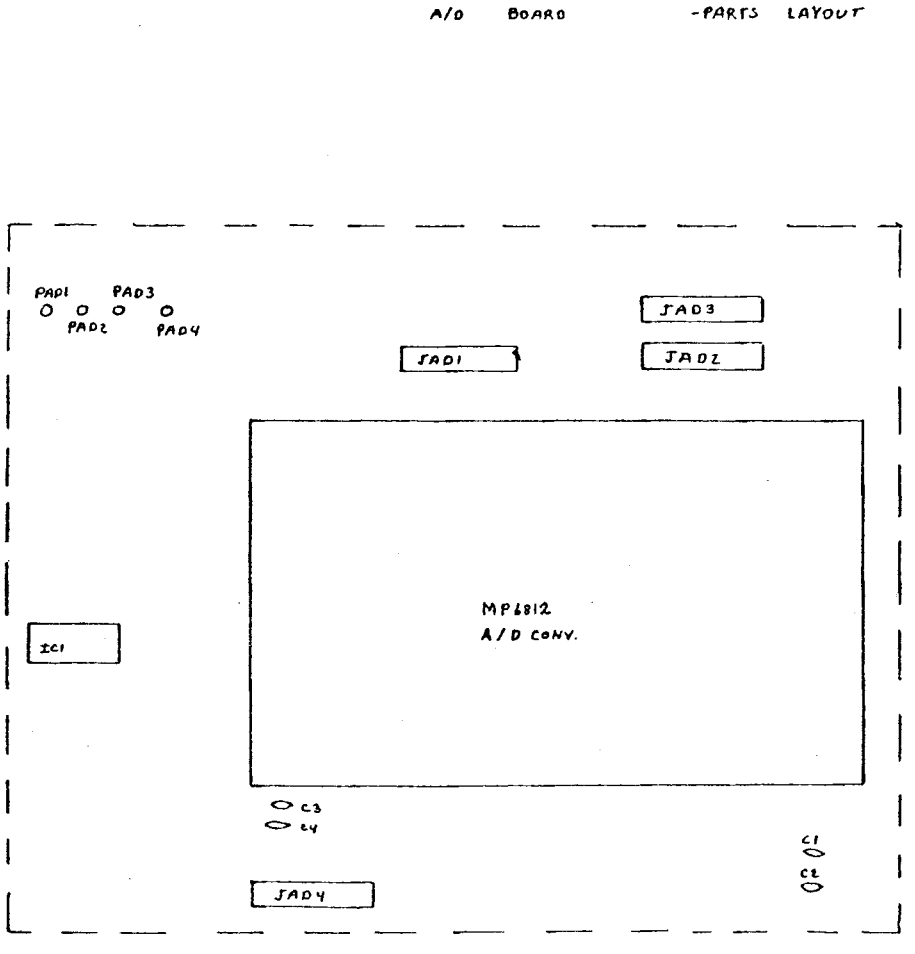

Figure A-31. A/D Converter Layout

PARTS LIST MULTIPLEXER BOARD

IC1-IC15	74C157	Quad 2-in. MUX
IC16, IC17	80C95	hex tri-state buffer
IC18, IC19	4N49	Texas Instrument, high gain opto-isolator
IC20	74C14	hex Schmidt trigger inverter
R1	1.3KΩ	1/4W 5% carbon
R2	5.1KΩ	1/4W 5% carbon
R3	1.3KΩ	1/4W 5% carbon
D1, D2	IN914	
T1	50KΩ	15 turn bourns 3006P Trimpot
T2-T4	100KΩ	15 turn bourns 3006P Trimpot

PARTS LIST CALCULATOR INTERFACE

IC1-4	74C157	Quad 2-in mux
IC5,6	80C95	hex tri-state buffer
IC7	74C221	Dual one shot
IC8,9	TMS25L32JDL	Texas Instruments 32K EPROM
IC10	74C00	Quad 2-in NAND
IC11	74C32	Quad 2-in NOR
IC12	74C08	Quad 2-in AND
IC13	-	Not used
IC14	74C83	4-bit full adder
IC15-17	80C95	hex tri-state buffer
R1-6	100 kΩ	¼ w 5% carbon resistor
C1,C2	.001 µf ceramic	
C3,C4	.1 µf ceramic	
C5	.01 µf ceramic	
C6	.1 µf ceramic	
C7,8	.01 µf ceramic	
C9,10	.1 µf ceramic	
C11,12	.01 µf ceramic	

PARTS LIST FRONT PANEL

S1	-	See S1 computer interface
S2 - S8	AML21BBA2BA	microswitch
RA1 - RA4	E100KΩJ01	Panasonic thin film resistor network
R1 - R7	100KΩ	1/4W 5% carbon
TS1	3-1-41-10-0-0-3	C & K Thumbwheel switch
TS2	3-3-41-10-0-0-3	C & K Thumbwheel switch

ADDITIONS TO COMPUTER INTERFACE

S1	PA-2000	Centralab 3-pole 4-position rotary switch
S2	46206LR	Switchcraft slide switch

PARTS LIST COMPUTER INTERFACE

IC1	7404 hex inverter
IC2	7404 hex inverter
IC3	7414 hex inverter Schmidt trigger
IC4	74121 one shot
IC5	7402 Quad 2-in NOR Gate
IC6-IC13	HCPL-2731 Dual high gain opto couplers hp
IC14,IC15	6N139 high gain opto-coupler-hp
IC16	80C95 hex tri-state buffer
IC17	80C95 " " " "
IC18	80C95 " " " "
IC19	74C02 Quad 2-in NOR gate
IC20	74C221 Dual one shot
IC21	74C08 Quad 2-in and gate
D1,D2	IN914
D3	IN5820 Schottky power diode
C1	5 µf electrolytic
C2	.01 µf ceramic
C3	.01 µf ceramic
C4	.1 µf ceramic
C5	6.8 µf tantalum
C6	1500 pF ceramic
C7	.22 µf ceramic
C8	.1 µf film
C9	.1 µf ceramic
C10	.1 µf ceramic
C11	400 pF ceramic
R1-R17	1.8 K 1/4w carbon 5%
R18-R36	1K 1/4w carbon 5%
R37	.91k 1/4w carbon 5%
R38	51K 1/4w carbon 5%
R39	20K 1/4w carbon 5%
R40	200Ω 1/4w carbon 5%
R41	10Ω 1/4w carbon 5%
LED-1	LED220 T.I.
P1,P2	Semiconductor circuits 30 C 12-5S600 +5v 600 ma DC/DC converter
P3	Semiconductor circuits 30C12-15D100 ±15v 100 ma DC/DC converter

OBSERVATION COUNTER - PARTS LIST.

Board 1

IC1 ~ IC6	74C192	Decade counter
R1	100KΩ	1/4 carbon 5%
S1	8221	C & K pushbutton
S2	46206MR	switchcraft slide switch
C1	.01μF	ceramic
C2	.1μF	ceramic
TS1	3-6-41-10-0-0-3	C & K Thumbwheel switch
RA1-RA6	E100KΩJ01	Panasonic thinfilm resistor network
LCD	3918	Hamlin Display

Board 2

IC1 ~ IC4	74C151	8 channel digital MUX
D1 ~ 03	IN4734	5.6V Zener diode
C1, C2	.01μF	ceramic

MEMORY ADDRESS - PARTS IDENTIFICATION

BOARD 1.

IC1 ~ IC4	74C86	Quad XOR
LCD	596	Hamlin Display 3906-363-6

BOARD 2.

IC1 - IC4	74C86	Quad XOR

Board 3.

IC1	MC14495	BCD - 7 segment hex decoder/driven
IC2	74C193	Binary counter
IC3	MC14495	BCD - 7 segment hex decoder/driven
IC4	74C193	Binary counter
IC5	74C02	Quad NOR GATE
R1 ~ R17	100kΩ	1/4W carbon 5%
S1 ~ S4	8221	C & K pushbutton switch
TS1	29000 series	Digitran hexadecimal 4-station thumbwheel switch

Board 4.

IC1	MC14495	BCD-7segment hex decoder/driver
IC2	74C193	Binary counter
IC3	MC14495	BCD-7segment hex decoder/driver
IC4	74C193	Binary counter
IC5	74C221	Dual O/S
R1	10KΩ	1/4W carbon 5%
C1	.01μF	ceramic

TIME CLOCK - PARTS LIST

BOARD 1.

IC1 ~ IC4	CD4518BC	Dual decade counter
IC5	74C00	Quad NAND GATE
IC6	74C00	Quad NAND GATE
IC7	74C86	Quad Exclusive OR GATE
IC8	74C08	Quad AND GATE
R1 ~ R3	100KΩ	1/4W 5% carbon
S1 ~ S3	8631	C & K pushbutton switch
LCD	3918 - 363 - G	Hamlin display

BOARD 2.

IC1 ~ IC3	74C374	OCTAL LATCH
IC4, IC5	74C901	hex invertor buffer
IC6	74C74	Dual flip-flop
IC7	MM5369	17 stage divider
R1	10MΩ	1/4W 5% carbon
R2	1KΩ	1/4W 5% carbon
D1, D2, D4	IN914	
D3	IN5820	Schottky diode
C1, C2	30PF	ceramic

PARTS LIST LCD BOARD 1

IC1-IC3	EC4543BCN LCD Display driven
C1	.01 µf ceramic
LCD	Hamlin Model 3918 LCD 3918-363-6 (Requires 2 TI 40 pin WW sockets)

PARTS LIST LCD BOARD 2

IC1-IC3	CD4543BCN .01 µf ceramic (Requires 2 TI 40 pin WW sockets)

PARTS LIST A/D BOARD

IC1	74C157	Quad 2-in mux
MP6812DM		Data acquisition system vendor: Analogic Corp.
C1		.1μf ceramic
C2		15μf tantalum
C3, C4		.01μf ceramic

PARTS LIST CONTROLLER BOARD

IC1	-	Trimpots
IC2	74C221	Dual one-shot
IC3	74C221	Dual one-shot
IC4	74C85	4-bit comparator
IC5	74C157	Quad 2-in. MUX
IC6	-	Connector CC1
IC7	74C00	Quad 2-in. NAND
IC8	74C02	Quad 2-in. NOR
IC9	74C901	hex extended voltage inverter
IC10	74C32	Quad 2-in. OR
IC11	74C02	Quad 2-in. NOR
IC12	74C08	Quad 2-in. And
IC13	74C08	"
IC14	74C08	"
IC15	74C08	"
IC16	74C107	Dual J-K Flip Flop
IC17	74C32	Quad 2 in. OR
IC18	-	Connector CC2
IC19	74C32	Quad 2-in. OR
IC20	74C04	hex inverter
IC21	74C193	Synchronous 4-bit counter
IC22	74C02	Quad 2-in. NOR
IC23	74C08	Quad 2-in. And
IC24	74C902	hex extended voltage buffer
IC25	-	Trimpots
IC26	74L123 (NS)	low power dual one shot TTL
IC27	74C08	Quad 2-in. And
IC28	74C221	Dual one shot
IC29	74C902	hex extended voltage buffer
IC30	-	Connector pins PCC-9 through PCC-16
R1	30.1KΩ	1% RN60D metal film
R2	30.1KΩ	1% RN60D metal film
R3	24KΩ	1/4 W 10% carbon
R4	100KΩ	"
R5	133KΩ	1% RN60D

PARTS LIST CONTROLLER BOARD CON'T.

R6	133KΩ	1% RN60D METAL FILM
R7	1MΩ	¼W 5% CARBON
R8	24KΩ	¼W 5% CARBON
C1	250pF	CERAMIC
C2	250pF	CERAMIC
C3	200pF	CERAMIC
C4	1500pF	CERAMIC
C5	33pF	CERAMIC
C6	33pF	CERAMIC
C7	.1μF	CERAMIC
C8	200pF	CERAMIC
C9-C12	.01μF	CERAMIC
C13	.1μF	CERAMIC
T1	50K	BOURNS 3006P TRIMPOT
T2-T4	100K	BOURNS 3006P TRIMPOT
D1, D2	1N914	
S1, S3	46206LR	SWITCHCRAFT SLIDE SWITCH
S2	AML21BBA2BA	MICRO-SWITCH PUSHBUTTON SWITCH
TS1	SERIES 29000	DIGITRAN HEX SINGLE STATION THUMBWHEEL SWITCH

PARTS LIST MEMORY BOARDS (MEM-2)

QUANTITY	DESCRIPTION
32	1Kx4 STATIC RAM HITACHI P/N HM4334P-450
2	MM80C98 HEX TRI-STATE INVERTER
1	MM74C32 QUAD OR GATE
3	MM80C97 HEX TRI-STATE BUFFER
43	.01MF Ceramic disc capacitor
1	.1MF Ceramic disc capacitor
1	10MF Aluminum Electrolytic 50V
1	14 pin low profile socket
5	16 pin low profile socket
32	18 pin low profile socket

APPENDIX B

DEVICE SPECIFICATION SHEETS

~~(on request)~~

Send requests to:

Ms. Davida E. Parks
Laboratory for Applications
of Remote Sensing
Purdue University
1220 Potter Drive
West Lafayette, IN 47906 U.S.A.

APPENDIX C

CHAPTER 4
DR11-C APPLICATIONS

4.1 BASIC INTERFACE

Figure 4-1 illustrates a typical user's device interface, consisting of a basic control section and a data assembly register.

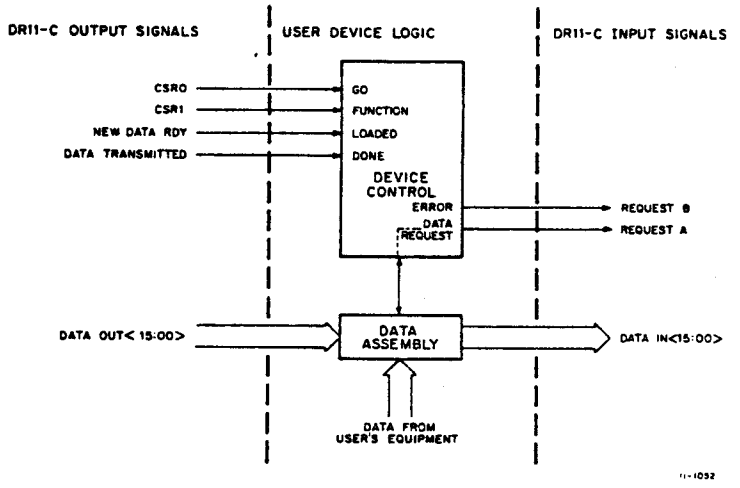

Figure 4-1 Basic Interface

Operation of the interface is initiated by the GO level. The FUNCTION bit informs the device whether it is to perform a read or write operation. When data is ready for transfer to the Unibus or data is required from the Unibus, a low-to-high transition on DATA REQUEST activates the REQUEST A line. The REQUEST A line initiates an interrupt sequence provided the INT ENB A bit in the DR11-C status register has been set. If the desired function is to load data into the user device, a LOADED (NEW DATA READY) pulse informs the device control when the data is ready for transfer. If a write function has been selected, a DONE (DATA TRANSMITTED) pulse informs the device control when the DR11-C has completed strobing of the data. The ERROR

line becomes true if some type of error condition occurs in the device. This ERROR line (REQUEST B) can either be monitored by the program or can be used to initiate an interrupt sequence (provided INT ENB B is set) to cause the program to branch to an error handling routine.

With the signals available to the user, there are many possible variations to this basic interface. For example, the two CSR bits (CSR0 and CSR1) could provide a 2-bit code to select one of four operations to be performed by the external device.

Another possibility would be to use one REQUEST line for interrupts and the other REQUEST line for a flag (associated INT ENB not used) in order to inform the program of the desired operation to be performed on the data.

A third possibility might be to use the two CSR bits as a selection code and have DONE (NEW DATA READY) serve as a start command so that device operation begins as soon as the DR11-C output buffer has been loaded from the bus.

4.2 INTERRUPT SERVICED INTERFACE

Figure 4-2 is an example of an interrupt serviced interface that employs a DR11-C to interface an analog-to-digital converter (ADC) to the Unibus. This interface allows the processor to concurrently execute instructions of another program while the ADC performs a cycle of operation. The processor responds to a READY (CONVERSION COMPLETE) signal from the ADC by interacting with the device and analyzing the data after it has been collected. This interface eliminates the necessity of having the processor spend time testing for a ready signal.

Note that this example uses only the REQUEST A line. The available REQUEST B line can be used as an ERROR indicator, if desired, and the two CSR lines could be used to initiate other actions within the external device.

A similar, and more detailed, example of this type of interface is given in the *PDP-11 Peripherals Handbook*. However, the example presented in this handbook uses a DR11-A which does not have all of the capabilities of the DR11-C interface.

4.3 GENERATING REQUEST LINE LEVELS

Two request lines (REQUEST A, B) are furnished and may be asserted (+3V) by the user's device to initiate an interrupt sequence or to produce a flag that can be tested by the program. The request lines must be levels and must remain asserted for the entire interrupt sequence. Typically, they are generated in the user's device by a REQUEST flip-flop which is set by the device when an interrupt is requested and cleared by the interrupt service routine by means of the NEW DATA READY or DATA TRANSMITTED signals.

Figure 4-3 represents the control circuit necessary to generate the REQUEST A H and REQUEST B H signals. Similar logic could be used if it is desired to have CSR0 H and CSR1 H control the clearing of the REQUEST lines.

4.4 INTERPROCESSOR BUFFER

Two DR11-C interfaces can be interconnected to allow data transfers and intercommunication between two PDP-11 Systems. Figure 4-4 is a simplified diagram of this interconnection.

The two interconnecting cables are the same as the MAINT cable and may be procured in either 1-ft or 25-ft lengths. Maximum allowable cable length is 25 ft.

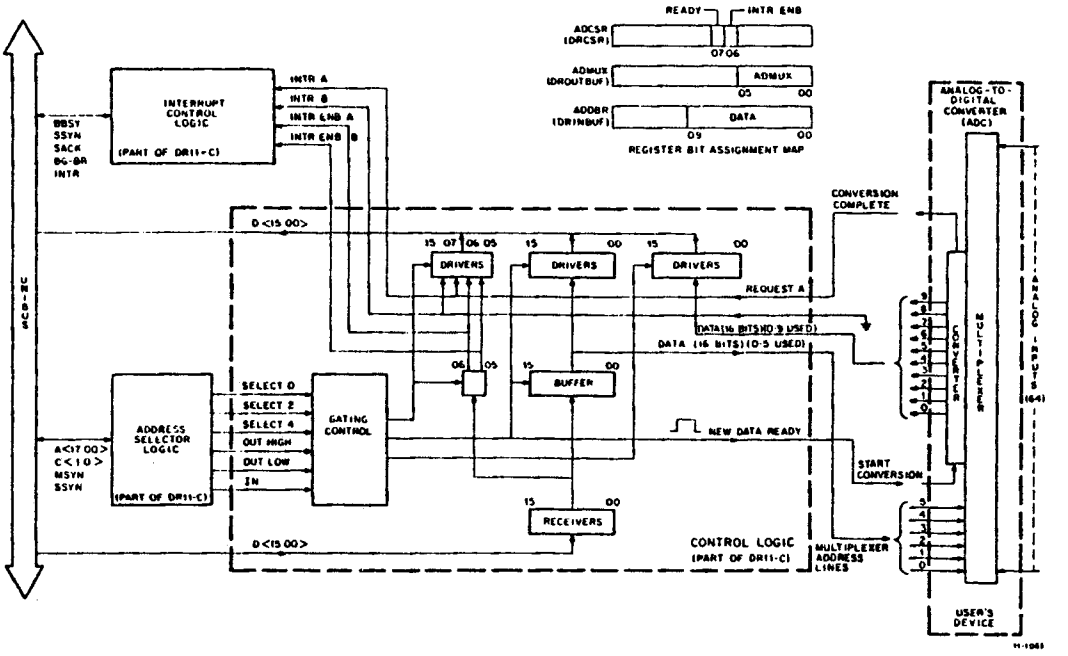

Figure 4-2 Interrupt Serviced Interface

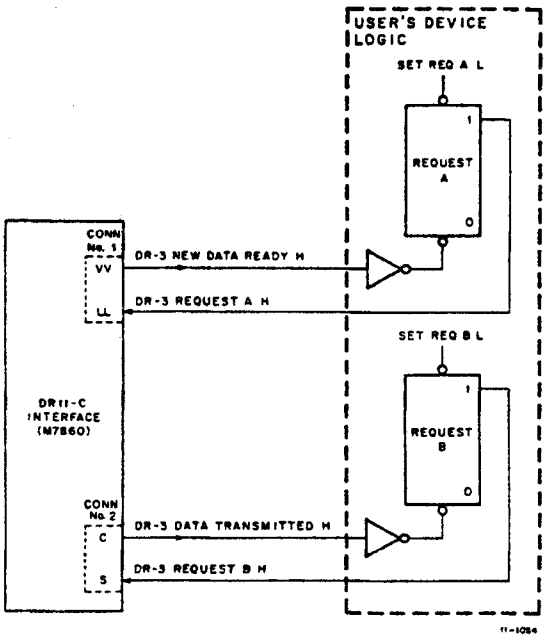

Figure 4-3 Request Line Control Logic

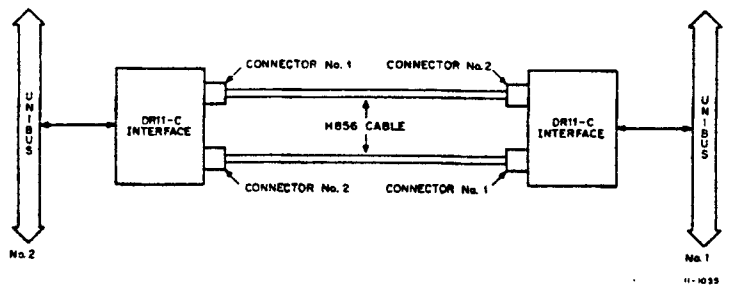

Figure 4-4 Interprocessor Buffer, Simplified Diagram

The Connector No. 1 of the first DR11-C is connected to Connector No. 2 of the second DR11-C This causes all of the output lines (OUT00 – OUT15) of the first interface to be connected to the corresponding input lines (IN00 – IN15) of the second interface (refer to pin connections given in Table 3-5). The CSR0 and CSR1 lines of the first unit are connected to the REQ A and B lines, respectively, of the second unit.

Connector No. 2 of the first unit is connected to Connector No. 1 of the second unit. This connects the IN lines and REQ lines of the first unit to the OUT lines and CSR lines of the second unit.

With the two PDP-11 buses interfaced in this manner, setting a CSR bit in one interface activates the REQ line in the other interface to initiate an interrupt sequence. Data can then be loaded from the bus into the DROUTBUF of the first unit for transfer to the DRINBUF of the second unit.

When DR11-Cs are used as interprocessor buffers, a power fail situation on either Unibus must be handled by the software. The software routine would be entered from the power fail trap vector and, by use of the REQUEST lines, would inform the other DR11-C that power is failing.