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HETERARCHICAL ARCHITECTURES FOR PARALLEL PROCESSING OF DIGITAL IMAGES

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A novel architecture is proposed, suitable for high-speed digital processing of LANDSAT and other pictures. The machine comprises a collection (20 to 100) of small active units, perhaps microprocessors, each of them performing a task on a subimage. The coordination between them is handled by a blackboard or dispatcher. This is a memory that contains addresses of tasks ready to be done, as well as destinations of the results of finished computations. The name "heterarchy" is used because there is no hierarchy of processors (active units).

The machine exhibits some form of graceful degradation, and is incrementally expandible.

The main components are: an image memory, where the image to be processed resides; the active units, which perform the work; the dispatcher or blackboard, which contains pointers to work yet to be done; and a universal bus that connects the machine to a general purpose computer, making it appear as a peripheral unit.

The machine is compared with a general purpose heterarchical machine.

The machine, if built, will enhance the data handling capabilities of the Proyecto P.R. at IIMAS-UNAM.

Key words: parallel computing; picture processing; heterarchy; graceful degradation; incrementally expandible; microprocessors.